Shanghai Fudan Microelectronics Group Company Limited

FM25Q64AI3

64M-BIT SERIAL FLASH MEMORY

Datasheet

Sep. 2024

Trademarks

1. Description

The FM25Q64AI3 is a 64M-bit (8M-byte) Serial Flash memory, with advanced write protection mechanisms. The FM25Q64AI3 supports the standard Serial Peripheral Interface (SPI) and Dual/Quad I/O. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data.

The FM25Q64AI3 can be programmed 1 to 256 bytes at a time, using the Page Program instruction. It is designed to allow either single Sector/Block at a time or full chip erase operation. The FM25Q64AI3 can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

2. Features

- **64Mbit of Flash memory**
  - 2048 uniform sectors with 4K-byte each
  - 128uniform blocks with 64K-byte each or
  - 256uniform blocks with 32K-byte each
  - 256 bytes per programmable page
- **Wide Operation Range**
  - 2.7V~3.6Vsingle voltage supply
  - Industrial temperature range
- **Serial Interface**
  - Standard SPI: CLK, CS#, DI, DO, WP#
  - Dual SPI: CLK, CS#, DQ0, DQ1, WP#
  - Quad SPI: CLK, CS#, DQ0, DQ1, DQ2, DQ3
  - Continuous READ mode support
  - Program/Erase Suspend and Resume support
  - Allow true XIP(execute in place) operation
- **High Performance**
  - Max FAST_READ clock frequency: 104MHz
  - Max READ clock frequency: 66MHz
  - Typical page program time: 0.4ms
  - Typical sector erase time: 30ms
  - Typical block erase time: 150/200ms
  - Typical chip erase time: 25s
- **Low Power Consumption**
  - Typical Deep Power Down current: <1μA
- **Security**
  - Software and hardware write protection
  - Lockable 4X256-Byte OTP security Pages
  - 64-Bit Unique ID for each device
  - Discoverable parameters(SFDP) register
- **High Reliability**
  - Endurance: 100,000 program/erase cycles
  - Data retention: 20 years
- **Green Package**
  - 8-pin SOP (150mil)
  - 8-pin SOP (208mil)
  - 8-pin TDFN(5×6mm)
  - 24-ball BGA (8x6mm) (5x5 Ball Array)
  - 8-pin USON (4x3mm)
  - All Packages are RoHS Compliant and Halogen-free

3. Packaging Type And Pin Configurations

FM25Q64AI3 is offered in an 8-pin SOP (150mil)，an 8-pin SOP (208mil)，an 8-pin TDFN (5x6mm)， a 8-pin USON (4x3mm) and a 24-ball BGA (8x6mm) packages as shown in Figure 1-5 respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

3.1. Pin Configuration SOP8 (150-mil) and SOP8 (208-mil)

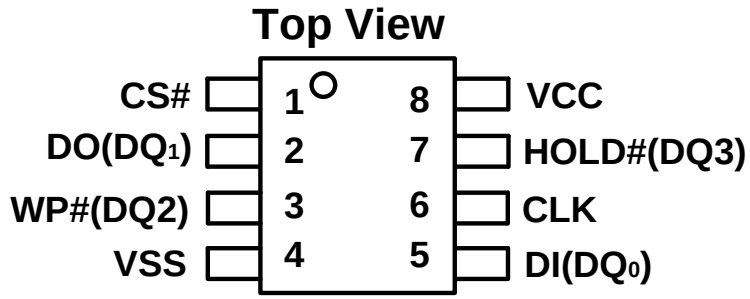


Figure 1 FM25Q64AI3 pin assignments, 8-pin SOP (150mil/ 208mil)

3.2. Pin Configuration TDFN8 (5x6mm) and USON8 (4x3-mil)

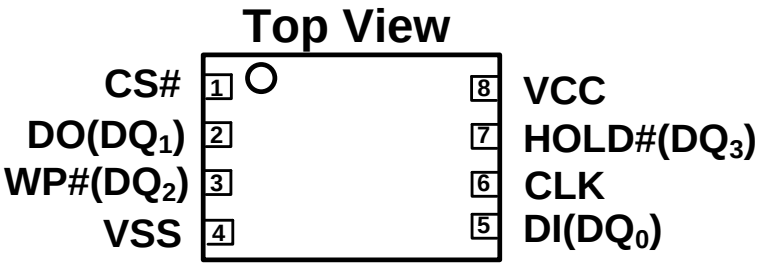


Figure 2 FM25Q64AI3 pin assignments, 8-pin TDFN (5x6mm) and USON (4x3mm)

3.3. Pin Configuration BGA24 (8x6mm)

BGA24(8x6mm) 5x5 ball array

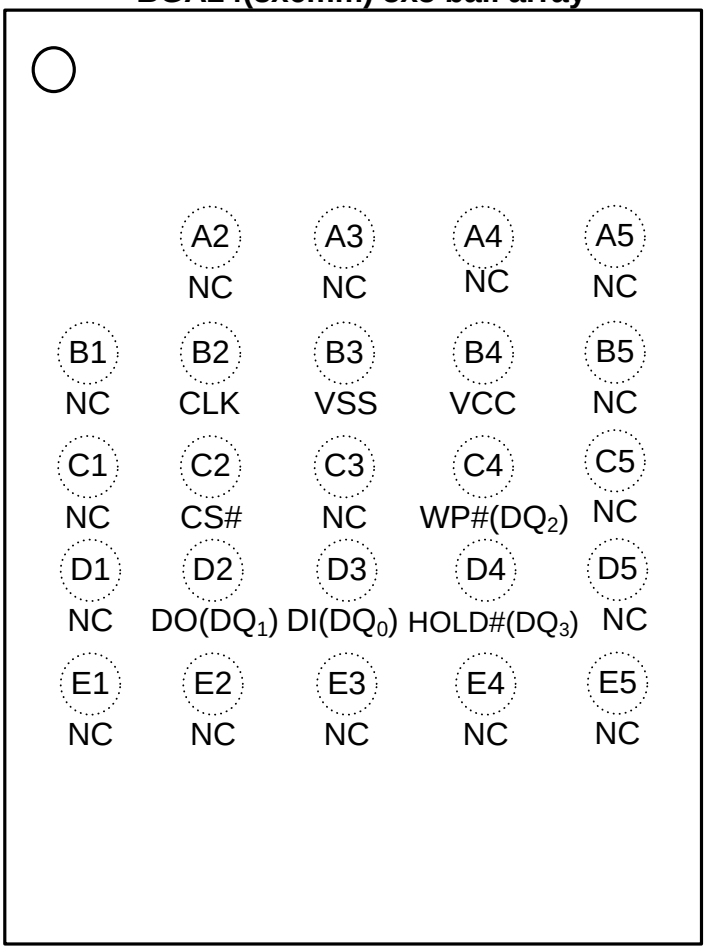


Figure 3 FM25Q64AI3 pin assignments, 24-ball BGA(8x6mm)

3.4. Pin Configurations

PIN NAME	I/O	FUNCTION
CS#	I	Chip Select Input
DO (DQ_1)	I/O	Data Output (Data Input Output 1)[1]
WP# (DQ_2)	I/O	Write Protect Input (Data Input Output 2)[2]
VSS		Ground
DI (DQ_0)	I/O	Data Input (Data Input Output 0)[1]
CLK	I	Serial Clock Input
HOLD# (DQ_3)	I/O	Hold Input (Data Input Output 3)[2]
VCC		Power Supply

Note:
1 DQ0 and DQ1 are used for Dual SPI instructions.
2 DQ0 – DQ3 are used for Quad SPI instructions.

4. Block Diagram

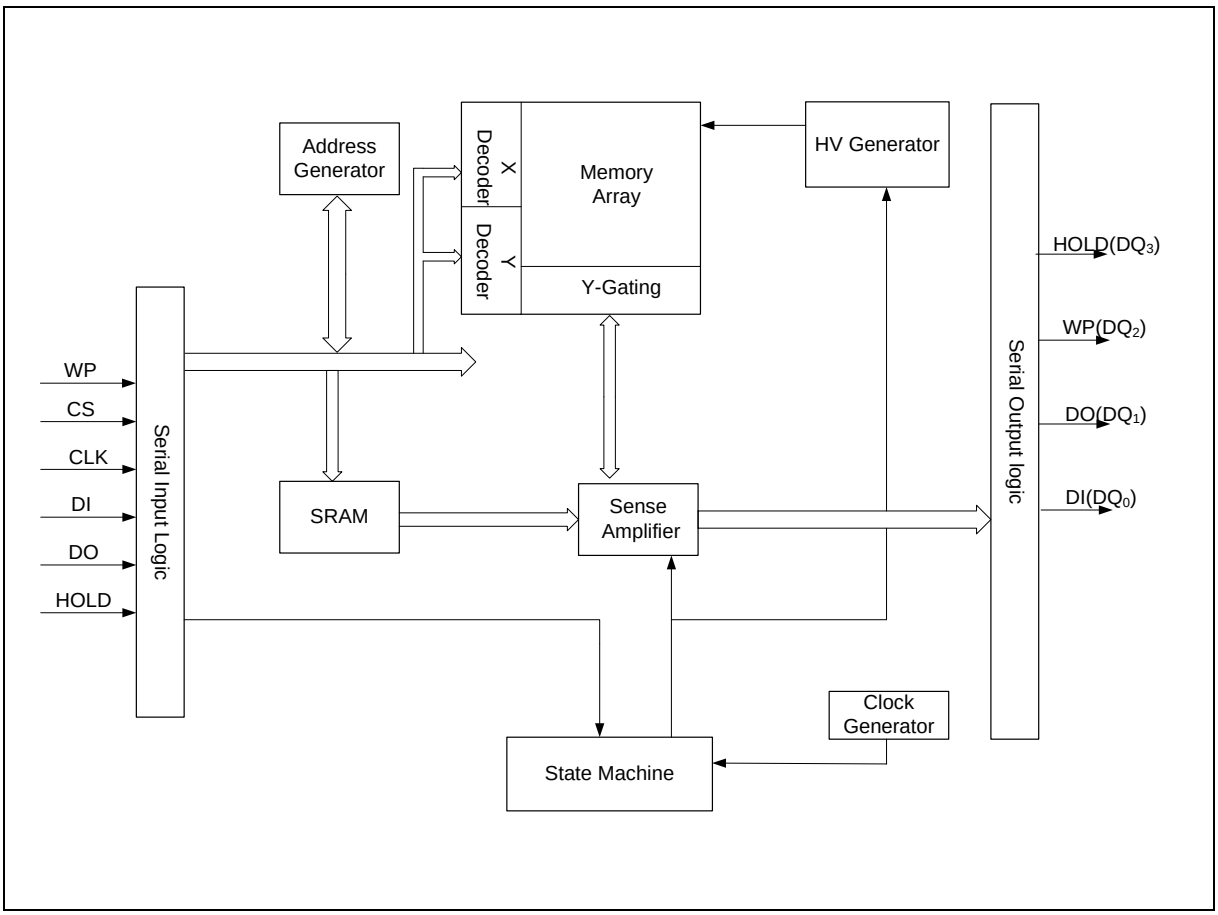


Figure 4 FM25Q64AI3 Serial Flash Memory Block Diagram

5. Pin Descriptions

Serial Clock (CLK): The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

Serial Data Input, Output and I/Os (DI, DO and DQ_0, DQ_1, DQ_2, DQ_3): The FM25Q64AI3 supports standard SPI, Dual SPI, Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual/Quad SPI instructions use the bidirectional DQ pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.When QE=1, the WP# pin becomes DQ_2 and HOLD# pin becomes DQ_3.

Chip Select (CS#): The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high, the device is deselected and the Serial Data Output (DO, or DQ_0, DQ_1, DQ_2, DQ_3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When CS# is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted. The CS# input must track the VCC supply level at power-up (see “8Write Protection” and Figure 47). If needed a pull-up resister on CS# can be used to accomplish this. The CS# input must be pulled up in standby mode.

HOLD (HOLD#): The HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When HOLD# is brought high, device operation can resume. The HOLD# function can be useful when multiple devices are sharing the same SPI signals. The HOLD# pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the HOLD# pin function is not available since this pin is used for DQ_3.

Write Protect (WP#): The Write Protect (WP#) pin can be used to prevent the Status Registers from being written. Used in conjunction with the Status Register’s Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The WP# pin is active low. However, when the QE bit of Status Register-2 is set for Quad I/O, the WP# pin function is not available since this pin is used for DQ_2.

6. Memory Organization

The FM25Q64AI3 array is organized into 32,768 programmable pages of 256-bytes each. Up to 256 bytes can be programmed (bits are programmed from 1 to 0) at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase).The FM25Q64AI3 has 2,048 erasable sectors, 256 erasable 32-k byte blocks and 128 erasable 64-k byte blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage.

Table 1 Memory Organization

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
127	255 | 254	2047	7FF000h	7FFFFFh
		…	…	…
		2032	7F0000h	7F0FFFh
126	253 | 252	2031	7EF000h	7EFFFFh
		…	…	…
		2016	7E0000h	7E0FFFh
125	251 | 250	2015	7DF000h	7DFFFFh
		…	…	…
		2000	7D0000h	7D0FFFh
…	…	…	…	…
		…	…	…
		…	…	…
…	…	…	…	…
		…	…	…
		…	…	…
2	5 | 4	47	02F000h	02FFFFh
		…	…	…
		32	020000h	020FFFh
1	3 | 2	31	01F000h	01FFFFh
		…	…	…
		16	010000h	010FFFh
0	1 | 0	15	00F000h	00FFFFh
		…	…	…
		2	002000h	002FFFh
		1	001000h	001FFFh
		0	000000h	000FFFh

7. Device Operations

7.1. Standard SPI

The FM25Q64AI3 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

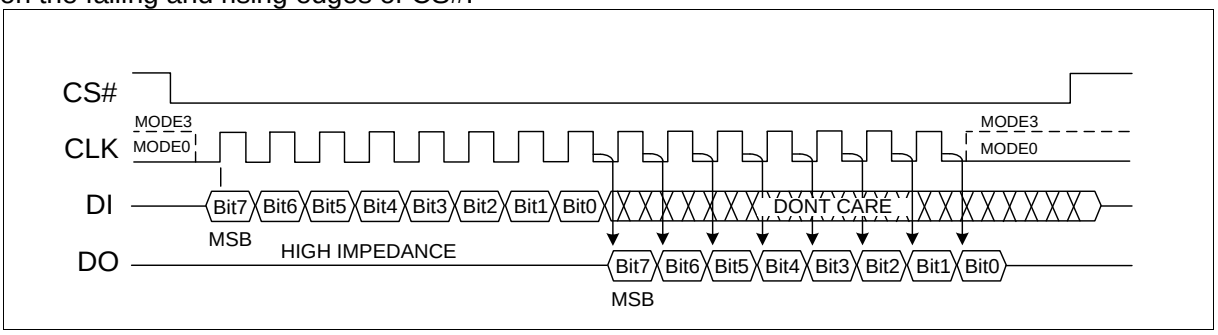


Figure 5 The difference between Mode 0 and Mode 3

7.2. Dual SPI

The FM25Q64AI3 supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed- critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: DQ_0 and DQ_1.

7.3. Quad SPI

The FM25Q64AI3 supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)”, “Word Read Quad I/O (E7h)” and “Octal Word Read Quad I/O (E3h)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional DQ_0 and DQ_1 and the WP # and HOLD# pins become DQ_2 and DQ_3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

7.4. Hold

For Standard SPI and Dual SPI operations, the HOLD# signal allows the FM25Q64AI3 operation to be paused while it is actively selected (when CS# is low). The HOLD# function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the

SPI bus. In this case the HOLD# function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The HOLD# function is only available for standard SPI and Dual SPI operation, not during Quad SPI.

To initiate a HOLD# condition, the device must be selected with CS# low. A HOLD# condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will activate after the next falling edge of CLK. The HOLD# condition will terminate on the rising edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will terminate after the next falling edge of CLK. During a HOLD# condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the HOLD# operation to avoid resetting the internal logic state of the device.

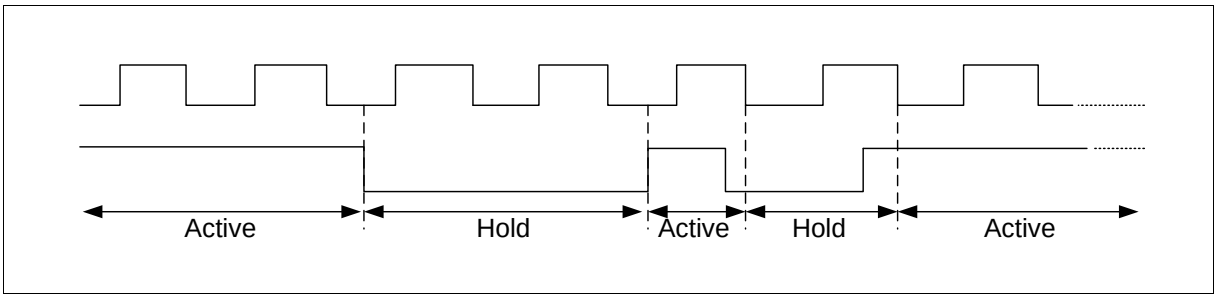


Figure 6 Hold Condition Waveform

8. Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the FM25Q64AI3 provides several means to protect the data from inadvertent writes.

Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (WP# pin) write protection using Status Register
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write protection for array and Security Sectors using Status Register.

Upon power-up or at power-down, the FM25Q64AI3 will maintain a reset condition while VCC is below the threshold value of VWI, (See “11.3Power-up Timing” and Figure 47). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds VWI, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (CS#) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached. If needed a pull-up resister on CS# can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits. These settings allow a portion as small as a 4KB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (WP#) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

9. Status Register

The Read Status Register instructions can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Sector lock status. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting and Security Sector OTP lock. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and during Standard/Dual SPI operations, the WP# pin.

Factory default for all Status Register bits are 0.

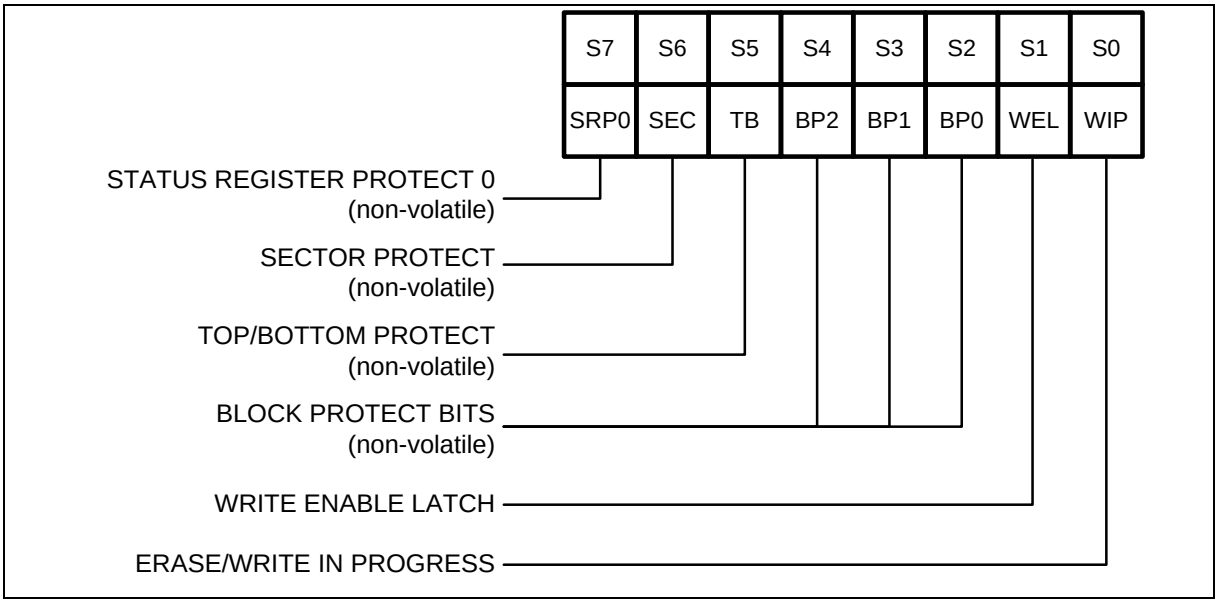


Figure 7 Status Register-1

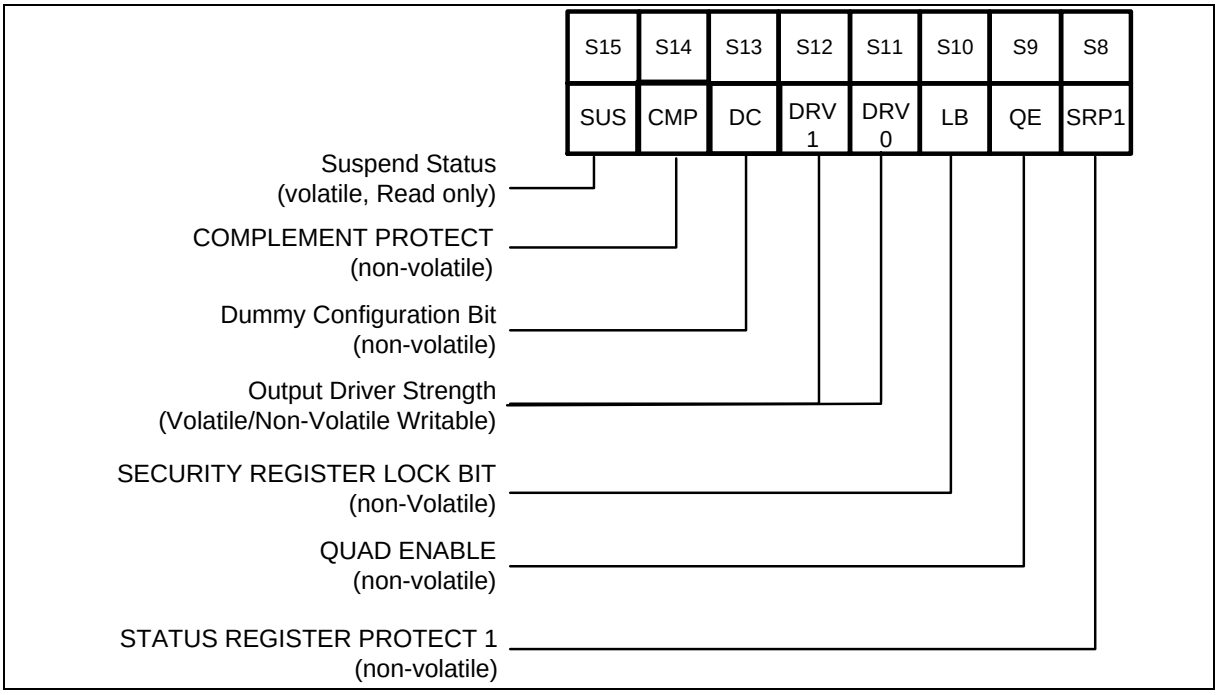


Figure 8 Status Register-2

9.1. WIP Bit

WIP is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Sector instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see t_W, t_{PP}, t_{SE},t_{BE}, and t_{CE} in “11.6AC Electrical Characteristics”). When the program, erase or write status register(or security sector)instruction has completed, the WIP bit will be cleared to a 0 state indicating the device is ready for further instructions.

9.2. Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Sector and Program Security Sector.

9.3. Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see t_W in “11.6AC Electrical Characteristics”). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Table 3Status Register Memory Protection). The factory default setting for the Block Protection Bits is 0, none of the array protected.

9.4. Top/Bottom Block Protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in Table 3Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

9.5. Sector/Block Protect (SEC)

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in Table 3Status Register Memory Protection table. The default setting is SEC=0.

9.6. Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 4KB sector can be protected while the rest of the array is not; when CMP=1, the top 4KB sector will become unprotected while the rest of the array become read-only. Please refer to Table 3Status Register Memory Protection table for details. The default setting is CMP=0.

9.7. Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8andS7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

Table 2 Status Register Protect bits

SRP1	SRP0	WP#	Status Register	Description
0	0	X	Software Protection	WP# pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. (Factory Default)
0	1	0	Hardware Protected	When WP# pin is low the Status Register locked and can not be written to.
0	1	1	Hardware Unprotected	When WP# pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down	Status Register is protected and can not be written to again until the next power-down, power-up cycle.(1)
1	1	X	One Time Program	Status Register is permanently protected and can not be written to.

Note:

1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.

9.8. Output driver strength (DRV1, DRV0)

The DRV1 & DRV0 bits are used to determine the output driver strength.

DRV1, DRV0	Driver Strength
0,0	100%
0,1	75%
1,0	50%
1,1	25%

9.9. Erase/Program Suspend Status (SUS)

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

9.10. Dummy Configuration (DC) Bit

The Dummy Configuration (DC) bit is non-volatile, which selects the number of dummy cycles between the end of address and the start of read data output. Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system. Some read commands require additional dummy cycles as the SCLK frequency increases.

The following dummy cycle tables provide different cycle settings that are configured.

Command	DC bit	Number of Dummy Cycles	Freq.(MHz)
BBH	0(default)	4	104

Command	DC bit	Number of Dummy Cycles	Freq.(MHz)
	1	8	133R
EBH	0(default)	4	104
	1	8	104

Note:
1.“R” means VCC range=3.0V~3.6V.

9.11. Security Sector Lock Bit (LB)

The Security Register Lock Bit (LB) is non-volatile One Time Program (OTP) bit in Status Register (S10) that provides the write protect control and status to the Security Registers. The default state of LB is 0, Security Registers are unlocked. LB can be set to 1using the Write Status Register instruction. LB bit is One Time Programmable (OTP), once it’s set to 1, the Security Registers will become read-only permanently.

9.12. Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default), the WP# pin and HOLD# are enabled. When the QE bit is set to a 1, the Quad DQ_2 and DQ_3 pins are enabled, and WP# and HOLD# functions are disabled.

WARNING: If the WP# or HOLD# pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

9.13. Status Register Memory Protection

Table 3 Status Register Memory Protection

STATUS REGISTER						FM25Q64AI3 (64M-BIT) MEMORY PROTECTION			
CMP	SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
0	X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	0	1	126 and 127	7E0000h – 7FFFFFh	128KB	Upper 1/64
0	0	0	0	1	0	124thru127	7C0000h – 7FFFFFh	256KB	Upper 1/32
0	0	0	0	1	1	120 thru 127	780000h – 7FFFFFh	512KB	Upper 1/16
0	0	0	1	0	0	112 thru 127	700000h – 7FFFFFh	1MB	Upper 1/8
0	0	0	1	0	1	96 thru 127	600000h – 7FFFFFh	2MB	Upper 1/4
0	0	0	1	1	0	64 thru 127	400000h – 7FFFFFh	4MB	Upper 1/1
0	0	1	0	0	1	0 and 1	000000h – 01FFFFh	128KB	Lower 1/64
0	0	1	0	1	0	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/32
0	0	1	0	1	1	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/16
0	0	1	1	0	0	0 thru 15	000000h – 0FFFFFh	1MB	Lower 1/8
0	0	1	1	0	1	0 thru 31	000000h – 1FFFFFh	2MB	Lower 1/4
0	0	1	1	1	0	0 thru 63	000000h – 3FFFFFh	4MB	Lower 1/2
0	X	X	1	1	1	0 thru 127	000000h – 7FFFFFh	8MB	ALL
0	1	0	0	0	1	127	7FF000h – 7FFFFFh	4KB	U - 1/2048
0	1	0	0	1	0	127	7FE000h – 7FFFFFh	8KB	U - 1/1024
0	1	0	0	1	1	127	7FC000h – 7FFFFFh	16KB	U - 1/512
0	1	0	1	0	X	127	7F8000h – 7FFFFFh	32KB	U - 1/256
0	1	0	1	1	0	127	7F8000h – 7FFFFFh	32KB	U - 1/256
0	1	1	0	0	1	0	000000h – 000FFFh	4KB	L - 1/2048
0	1	1	0	1	0	0	000000h – 001FFFh	8KB	L - 1/1024
0	1	1	0	1	1	0	000000h – 003FFFh	16KB	L - 1/512
0	1	1	1	0	X	0	000000h –	32KB	L - 1/256

STATUS REGISTER						FM25Q64AI3 (64M-BIT) MEMORY PROTECTION			
CMP	SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
							007FFFh		
0	1	1	1	1	0	0	000000h – 007FFFh	32KB	L - 1/256
1	X	X	0	0	0	ALL	000000h – 7FFFFFh	ALL	ALL
1	0	0	0	0	1	0 thru 125	000000h – 7DFFFFh	8,064KB	Lower 63/64
1	0	0	0	1	0	0 and 123	000000h – 7BFFFFh	7,936KB	Lower 31/32
1	0	0	0	1	1	0 thru 119	000000h – 77FFFFh	7,680KB	Lower 15/16
1	0	0	1	0	0	0 thru 111	000000h – 6FFFFFh	7MB	Lower 7/8
1	0	0	1	0	1	0 thru 95	000000h – 5FFFFFh	6MB	Lower 3/4
1	0	0	1	1	0	0 thru 63	000000h – 3FFFFFh	4MB	Lower 1/2
1	0	1	0	0	1	2 thru 127	020000h – 7FFFFFh	8,064KB	Upper 63/64
1	0	1	0	1	0	4 thru 127	040000h – 7FFFFFh	7,936KB	Upper 31/32
1	0	1	0	1	1	8 thru 127	080000h – 7FFFFFh	7,680KB	Upper 15/16
1	0	1	1	0	0	16 thru 127	100000h – 7FFFFFh	7MB	Upper 7/8
1	0	1	1	0	1	32 thru 127	200000h – 7FFFFFh	6MB	Upper 3/4
1	0	1	1	1	0	64 thru 127	400000h – 7FFFFFh	4MB	Upper 1/2
1	X	X	1	1	1	NONE	NONE	NONE	NONE
1	1	0	0	0	1	0 thru 127	000000h – 7FEFFFh	8,188KB	L - 2047/2048
1	1	0	0	1	0	0 thru 127	000000h – 7FDFFFh	8,184KB	L - 1023/1024
1	1	0	0	1	1	0 thru 127	000000h – 7FBFFFh	8,176KB	L - 511/512
1	1	0	1	0	X	0 thru 127	000000h – 7F7FFFh	8,160KB	L - 255/256
1	1	0	1	1	0	0 thru 127	000000h – 7F7FFFh	8,160KB	L - 255/256
1	1	1	0	0	1	0 thru 127	001000h – 7FFFFFh	8,188KB	U - 2047/2048
1	1	1	0	1	0	0 thru 127	002000h – 7FFFFFh	8,184KB	U - 1023/1024
1	1	1	0	1	1	0 thru 127	004000h – 7FFFFFh	8,176KB	U - 511/512
1	1	1	1	0	X	0 thru 127	008000h – 7FFFFFh	8,160KB	U - 255/256
1	1	1	1	1	0	0 thru 127	008000h – 7FFFFFh	8,160KB	U - 255/256

10. Instructions

The Standard/Dual/Quad SPI instruction set of the FM25Q64AI3 consists of 35 basic instructions that are fully controlled through the SPI bus (see Table 5~Table 7Instruction Set). Instructions are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge CS#. Clock relative timing diagrams for each instruction are included in Figure 9 through Figure 51. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS# driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

10.1. Manufacturer and Device Identification

Table 4 Manufacturer and Device Identification

OP Code	MF7-MF0	ID15-ID0	ID7-ID0
ABh			16h
90h,92h,94h	A1h		16h
9Fh	A1h	4017h	

10.2. Standard SPI Instructions Set

Table 5 Standard SPI Instructions Set [1]

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*
Write Enable	**06h**					
Volatile SR Write Enable	**50h**					
Write Disable	**04h**					
Read Status Register-1	**05h**	(S7-S0)[2]				
Write Status Register-1	**01h**	S7-S0				
Read Status Register-2	**35h**	(S15-S8)[2]	01h can be used to program Status Register-1&2			
Write Status Register-2	**31h**	S15-S8				
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0[3]
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0		
Chip Erase	**C7h/60h**					
Power-down	**B9h**					
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Release Power down/ ID[4]	**ABh**	dummy	dummy	dummy	(ID7-ID0)[2]	
Manufacturer/Device ID[4]	**90h**	dummy	dummy	00h	(MF7-MF0)	(ID7-ID0)
JEDEC ID[4]	**9Fh**	(MF7-MF0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity		
Read SFDP Register	**5Ah**	00h	00h	A7-A0	dummy	(D7-D0)
Read Unique ID[5]	**4Bh**	dummy	dummy	dummy	dummy	(UID63-UID0)
Erase Security Sectors[6]	**44h**	A23-A16	A15-A8	A7-A0		
Program Security Sectors[6]	**42h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0[3]
Read Security Sectors[6]	**48h**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Program/Erase Suspend	**75h**					
Program/Erase Resume	**7Ah**					
Enable Reset	**66h**					
Reset	**99h**					

10.3. Dual SPI Instructions Set

Table 6 Dual SPI Instructions Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, …)(8)
Fast Read Dual I/O	**BBh**	A23-A8(7)	A7-A0, M7-M0 (7)	(D7-D0, …)(8)		
Manufacturer/Device ID by Dual I/O(4)	**92h**	A23-A8(7)	A7-A0, M7-M0(7)	(MF7-MF0, ID7-ID0)		

10.4. Quad SPI Instructions Set

Table 7 Quad SPI Instructions Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*
Quad Page Program	**32h**	A23-A16	A15-A8	A7-A0	D7-D0, …(10)	D7-D0, …(3)
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, …)(10)
Fast Read Quad I/O	**EBh**	A23-A0, M7-M0(9)	(xxxx, D7-D0)(11)	(D7-D0, …)(10)		
Set Burst with Wrap	**77h**	xxxxxx, W6-W4(9)				
Manufacture/Device ID by Quad I/O(4)	**94h**	A23-A0, M7-M0(9)	xxxx, (MF7-MF0, ID7-ID0)	(MF7-MF0, ID7-ID0, …)		

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data output from the device on either 1, 2 or 4 DQ pins.
2. The Status Register contents and Device ID will repeat continuously until CS# terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Sectors, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. See Table 4 Manufacturer and Device Identification for device ID information.
5. Please contact Shanghai Fudan Microelectronics Group Co., Ltd for details.
6. Security Sector Address:
   Security Sector: A23-A10 = 000h; A9-A8=00~11; A7-A0 = byte address
7. Dual SPI address input format:
   DQ_0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   DQ_1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
8. Dual SPI data output format:
   DQ_0 = (D6, D4, D2, D0)
   DQ_1 = (D7, D5, D3, D1)
9. Quad SPI address input format:
   DQ_0 = A20, A16, A12, A8, A4, A0, M4, M0
   DQ_1 = A21, A17, A13, A9, A5, A1, M5, M1
   DQ_2 = A22, A18, A14, A10, A6, A2, M6, M2
   Set Burst with Wrap input format:
   DQ_0 = x, x, x, x, x, x, W4, x
   DQ_1 = x, x, x, x, x, x, W5, x
   DQ_2 = x, x, x, x, x, x, W6, x

DQ_3 = A23, A19, A15, A11, A7, A3, M7, M3 DQ_3 = x, x, x, x, x, x, x, x

10. Quad SPI data input/output format:
    DQ_0 = (D4, D0, …)
    DQ_1 = (D5, D1, …..)
    DQ_2 = (D6, D2, …..)
    DQ_3 = (D7, D3, …..)
11. Fast Read Quad I/O data output format:
    DQ_0 = (x, x, x, x, D4, D0, D4, D0)
    DQ_1 = (x, x, x, x, D5, D1, D5, D1)
    DQ_2 = (x, x, x, x, D6, D2, D6, D2)
    DQ_3 = (x, x, x, x, D7, D3, D7, D3)

10.5. Write Enable (WREN) (06h)

The Write Enable (WREN) instruction (Figure 9) sets the Write Enable Latch (WEL) bit in the Status Register to a1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Sectors instruction. The Write Enable (WREN) instruction is entered by driving CS# low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

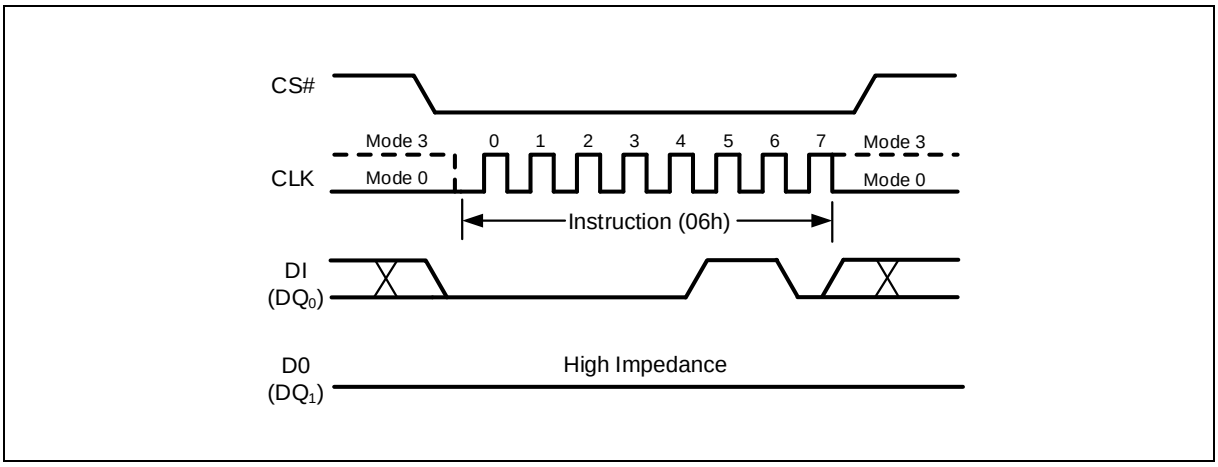


Figure 9 Write Enable Instruction for SPI Mode

10.6. Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 10.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h/31h) instruction. Write Enable for Volatile Status Register instruction (Figure 10) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

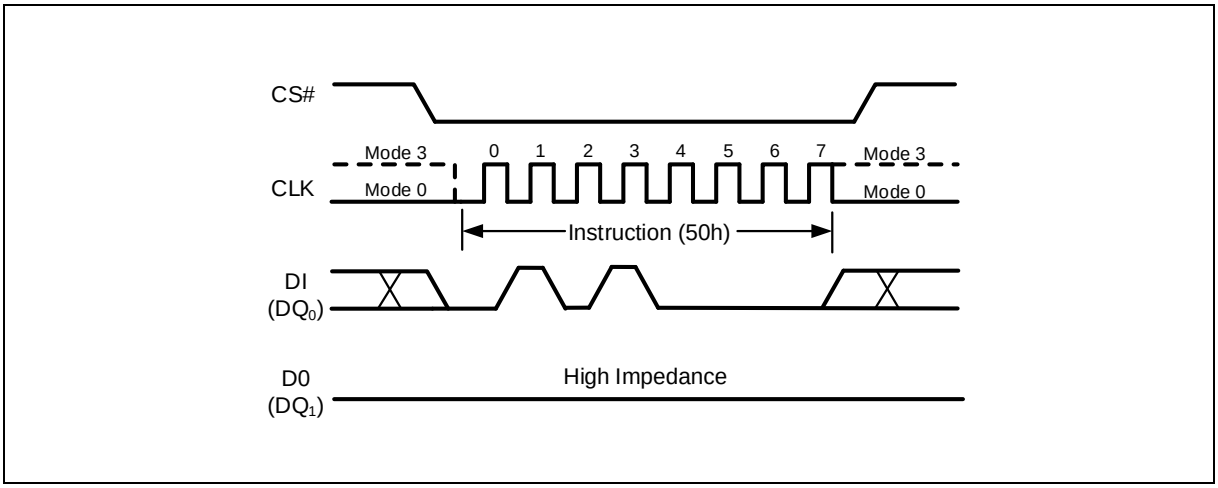


Figure 10 Write Enable for Volatile Status Register Instruction for SPI Mode

10.7. Write Disable (WRDI) (04h)

The Write Disable (WRDI) instruction (Figure 11) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable (WRDI) instruction is entered by driving CS# low, shifting the instruction code “04h” into the DI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Sectors, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset instructions.

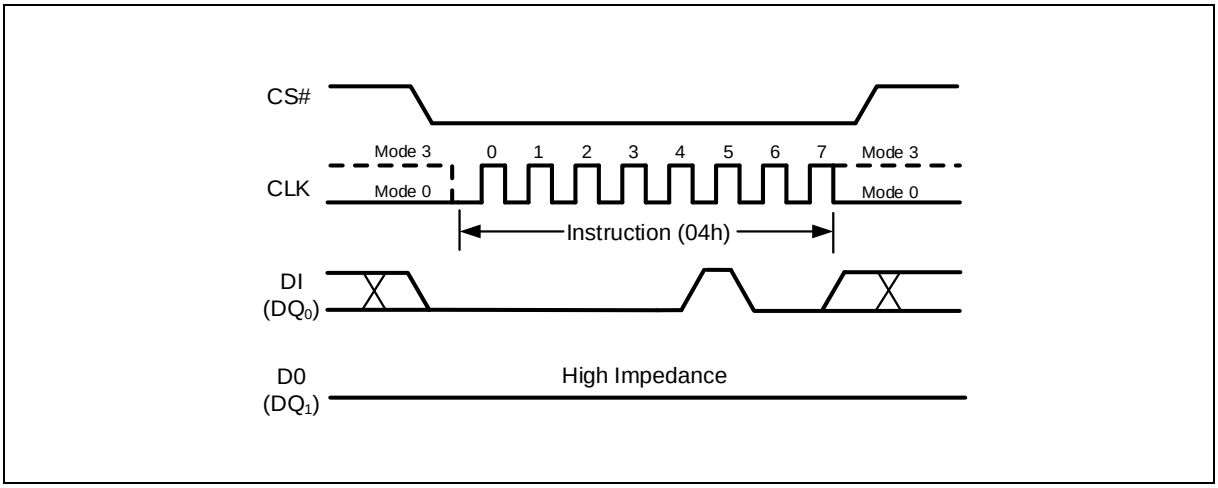


Figure 11 Write Disable Instruction for SPI Mode

10.8. Read Status Register-1(RDSR1) (05h), Status Register-2 (RDSR2)(35h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving CS# low and shifting the instruction code “05h”for Status Register-1 or “35h” for Status Register-2into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 12. The Status Register bits are shown in Figure 7andFigure 8.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the WIP status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 12The instruction is completed by driving CS# high.

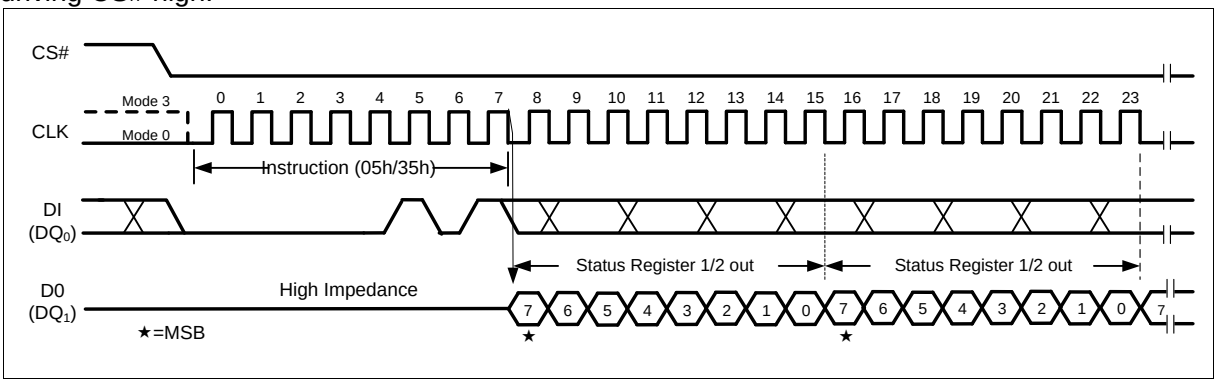


Figure 12 Read Status Register Instruction (SPI Mode)

10.9. Write Status Register-1(WRSR)(01h), Status Register-2 (31h)

The Write Status Register (WRSR) instruction allows the Status Register to be written. Only non-volatile Status Register bits SRP0, SEC, TB, BP2, BP1, BP0 (bits 7 thru 2 of Status Register-1) , CMP, DRV0, DRV1, LB, QE, SRP1 (bits 14 and bit 12 thru8 of Status Register-2) , can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register (WRSR) instruction. LB is non-volatile OTP bit, once it is set to 1, it cannot be cleared to 0. The Status Register bits are shown in shown in Figure 7andFigure 8and described in 9Status Register

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register(WRSR) instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in Figure 13 Write Status Register Instruction (SPI Mode).

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register (WRSR) instruction (Status Register bit WEL remains 0). However, SRP1 and LB, cannot be changed from “1” to “0” because of the OTP protection for these bits. Upon power off or the execution of a “Reset (99h)” instruction, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

To complete the Write Status Register (WRSR) instruction, the CS# pin must be driven high after the eighth or sixteenth bit of data that is clocked in. If this is not done the Write Status Register (WRSR) instruction will not be executed. If CS# is driven high after the eighth clock the DRV1, DRV0, CMP and QE bits will be cleared to 0.

During non-volatile Status Register write operation (06h combined with 01h), after CS# is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_W (See "11.6AC Electrical Characteristics"). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h), after CS# is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2}(See "11.6AC Electrical Characteristics"). WIP bit will remain 0 during the Status Register bit refresh period.

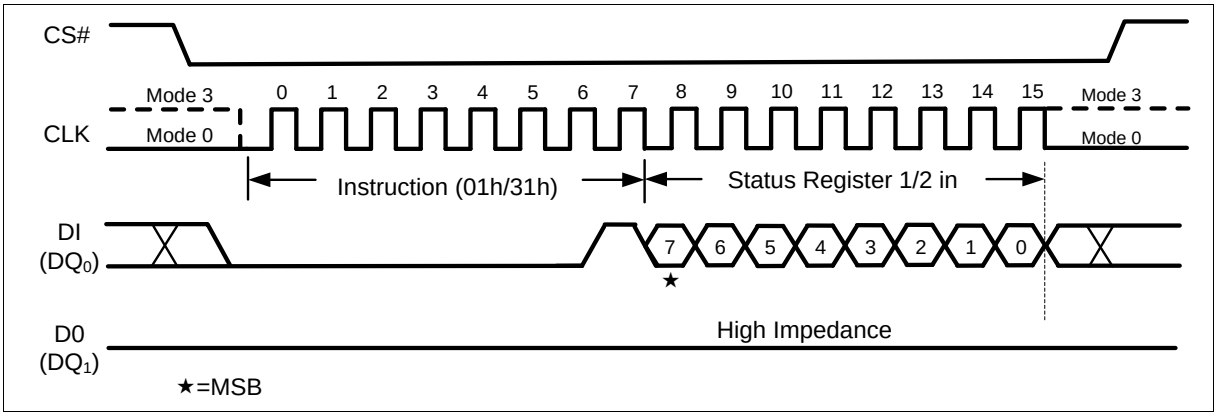


Figure 13 Write Status Register Instruction (SPI Mode)

The FM25Q64AI3 is also backward compatible to FMSH's previous generations of serial flash memories, in which the Status Register-1&2 can be written using a single "Write Register-1(01h)" command. To complete the Write Status Register1&2, the CS# pin must be driven high after the sixteenth bit of data that is clocked in as shown in Figure 14. If CS# is driven high after the eighth clock, the Write Status Register (WRSR)instruction will only program the Status Register-1, the Status Register-2 will not be affected.

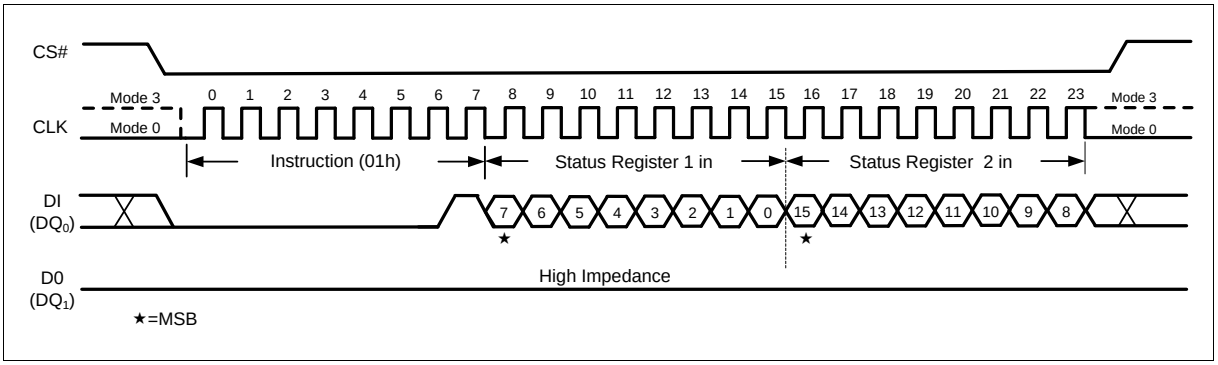


Figure 14 Write Status Register-1/2 Instruction (backward compatible, SPI Mode)

10.10. Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “03h” followed by a24-bit address A23-A0 into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving CS# high.

The Read Data instruction sequence is shown in Figure 15. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (WIP =1) the instruction is ignored and will not have any effect on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see“11.6AC Electrical Characteristics”).

The Read Data (03h) instruction is only supported in Standard SPI mode.

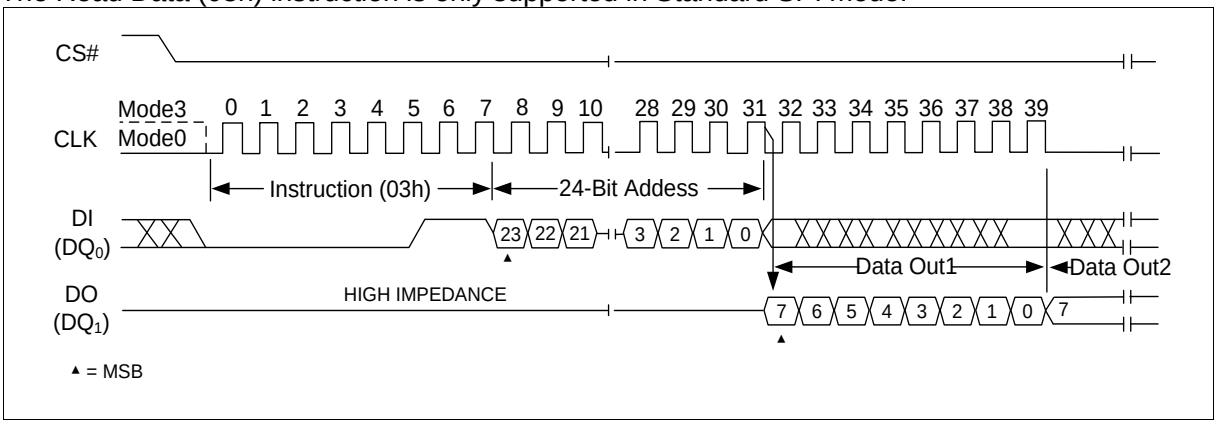


Figure 15 Read Data Instruction (SPI Mode)

10.11. Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of F_R (see "11.6AC Electrical Characteristics"). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 16. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DI pin is a "don't care".

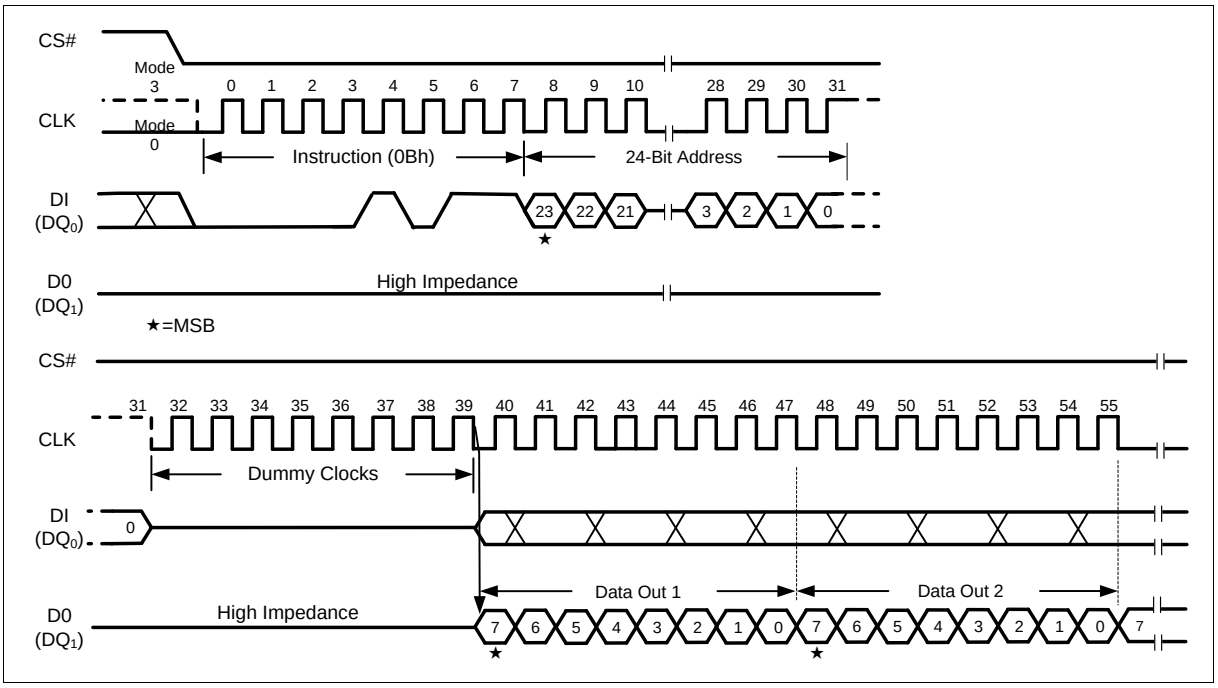


Figure 16 Fast Read Instruction (SPI Mode)

10.12. Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; DQ_0 and DQ_1. This allows data to be transferred from the FM25Q64AI3 at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of F_R(see “11.6AC Electrical Characteristics”). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 17. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the DQ_0 pin should be high-impedance prior to the falling edge of the first data out clock.

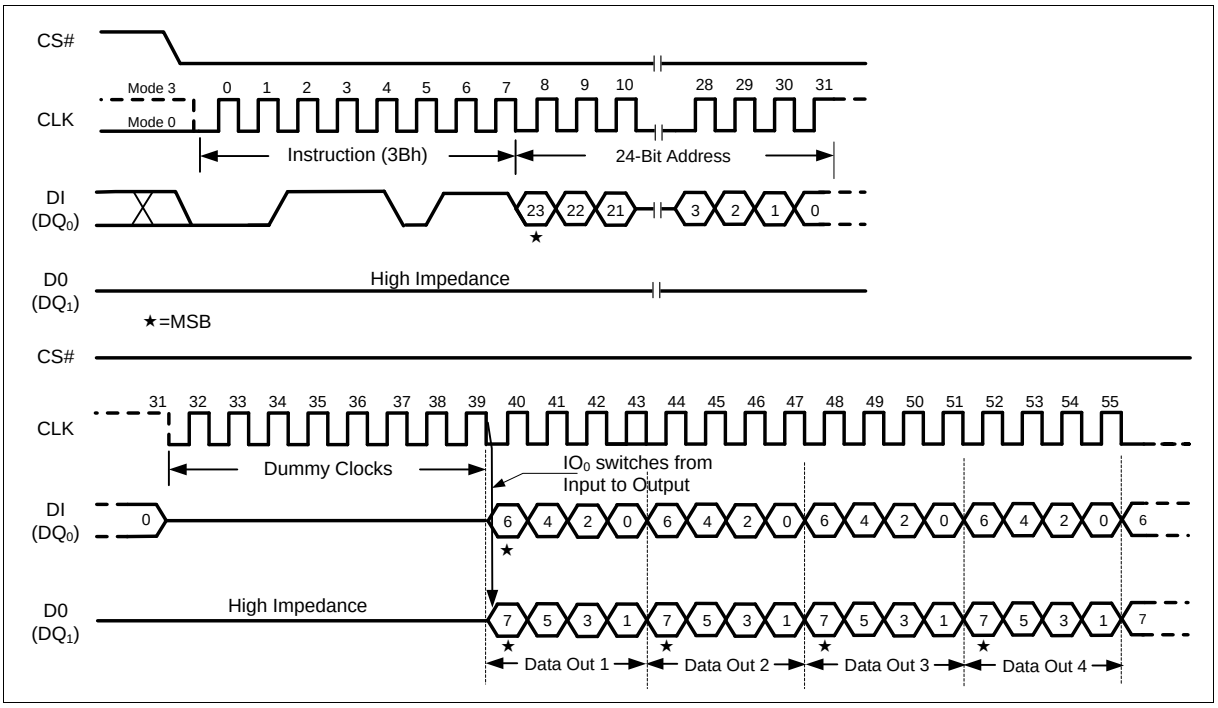


Figure 17Fast Read Dual Output Instruction (SPI Mode)

10.13. Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, DQ_0, DQ_1, DQ_2, and DQ_3. A Quad enable of Status Register-2 must be executed before the device will accept the Fast Read Quad Output Instruction (Status Register bit QE must equal 1).The Fast Read Quad Output Instruction allows data to be transferred from the FM25Q64AI3 at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of F_R (see "11.6AC Electrical Characteristics"). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 18. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

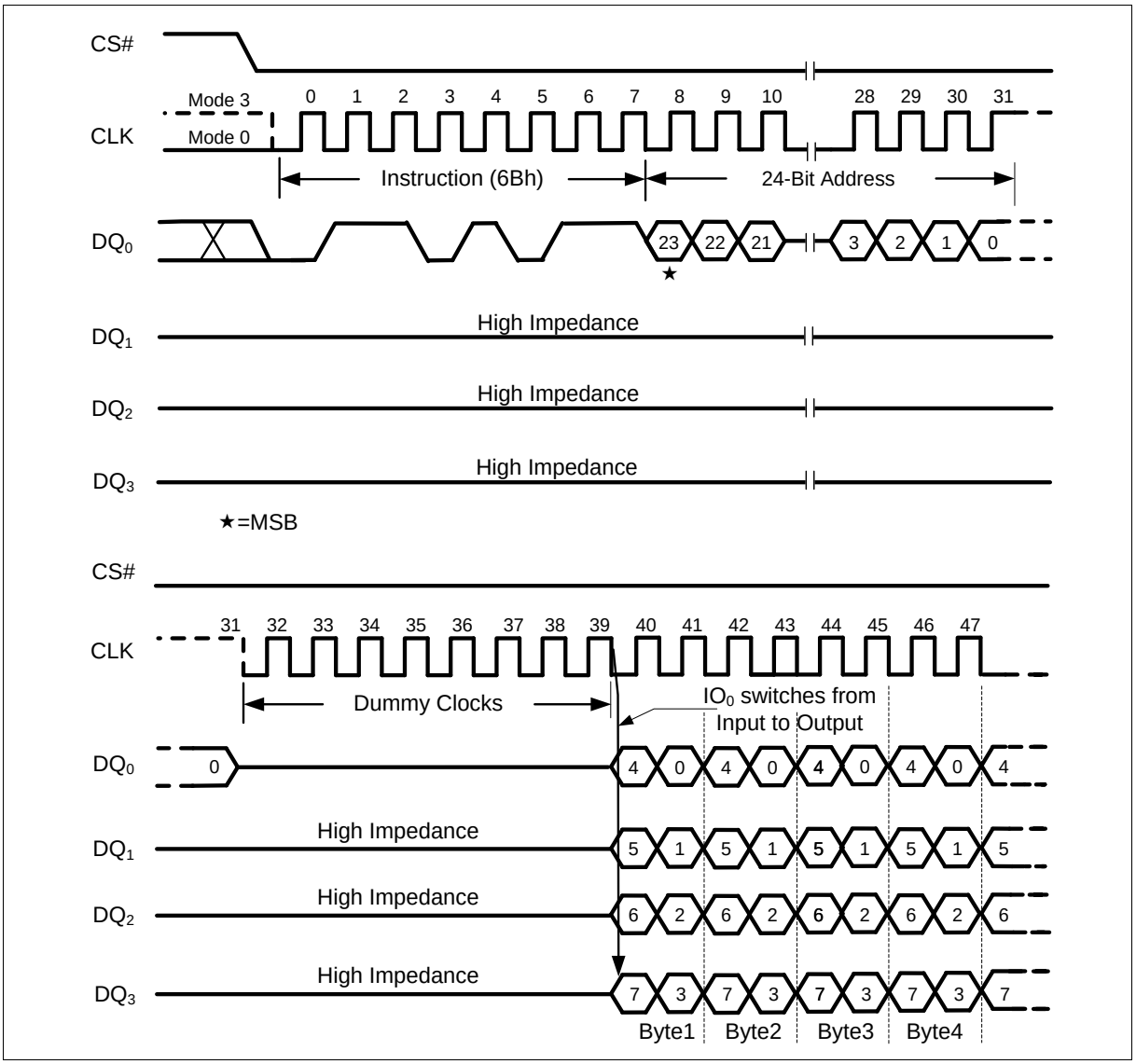


Figure 18 Fast Read Quad Output Instruction (SPI Mode)

10.14. Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two I/O pins, DQ_0 and DQ_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits A23-A0 two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits A23-A0, as shown in Figure 19. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after CS# is raised and then lowered) does not require the BBh instruction code, as shown in Figure 20. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on DQ_0 for the next instruction (8 clocks), to ensure M4= 1 and return the device to normal operation.

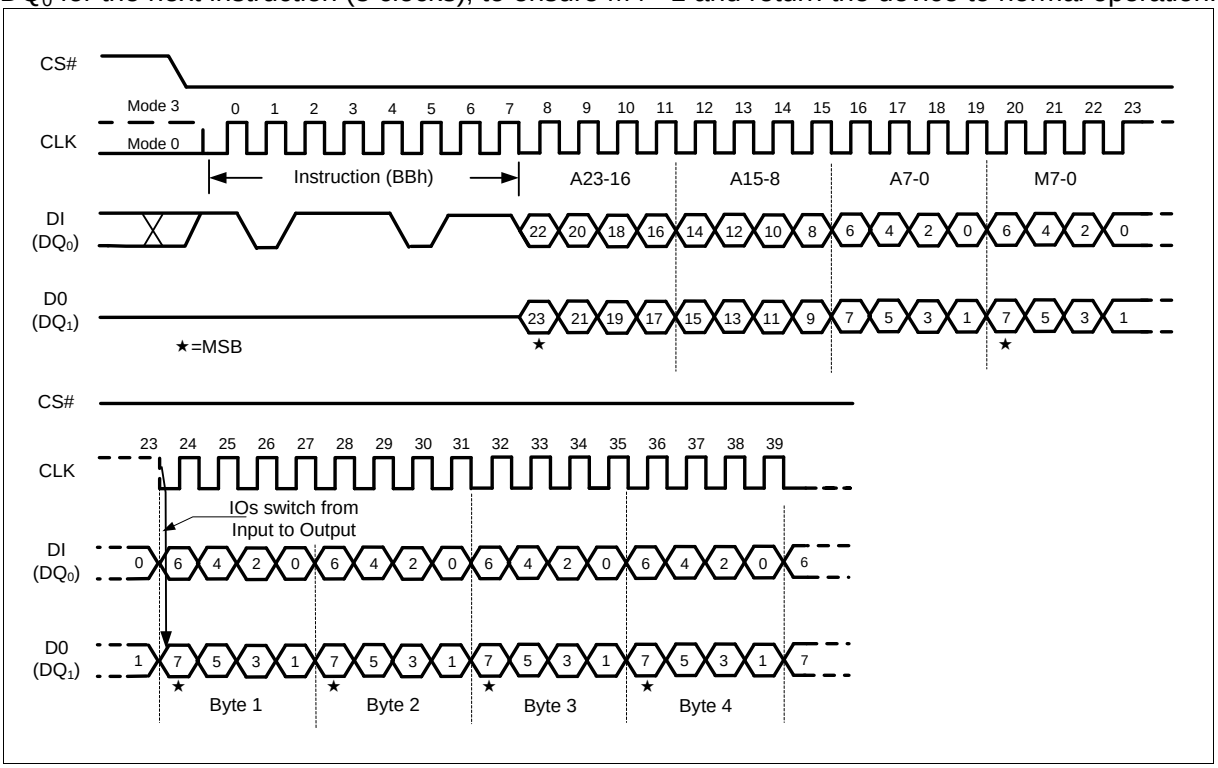


Figure 19 Fast Read Dual I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode)

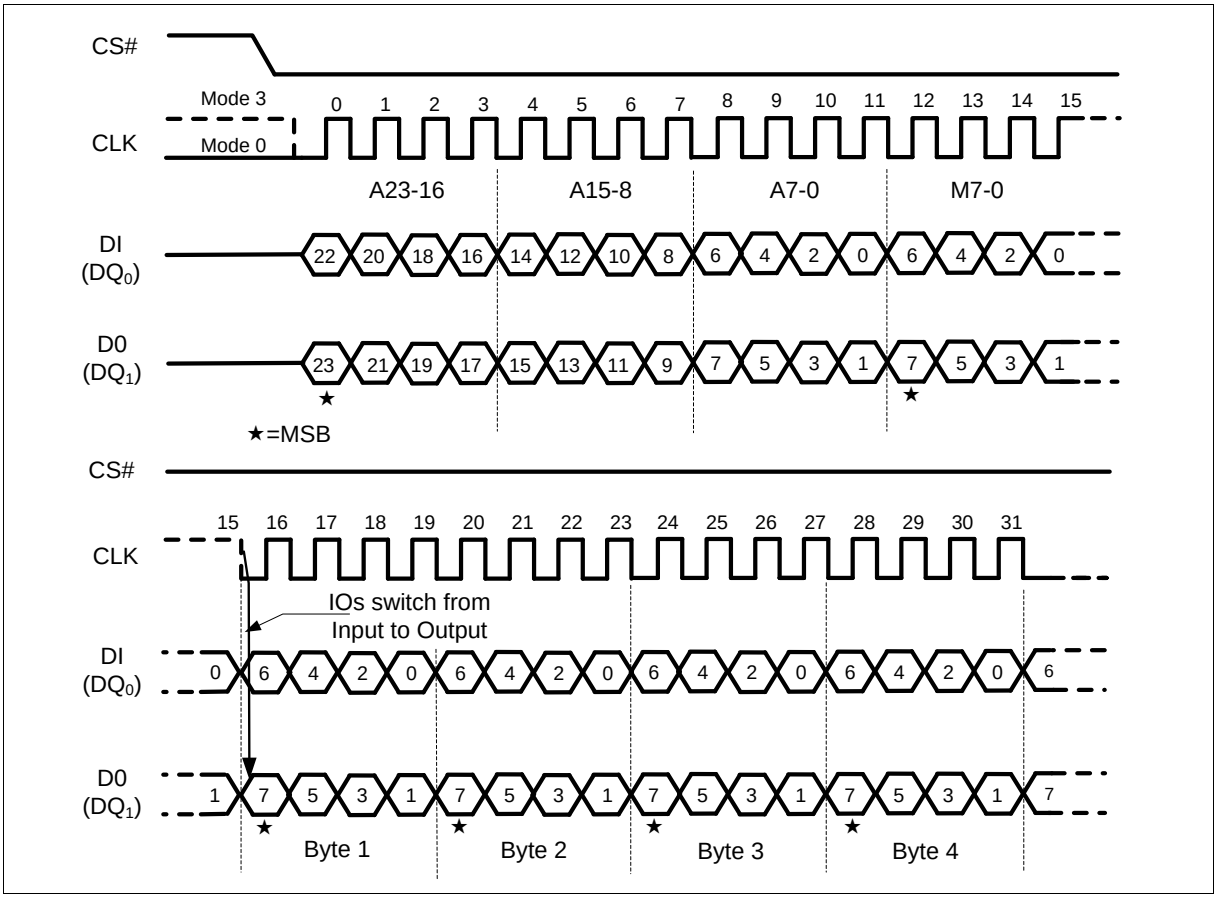


Figure 20 Fast Read Dual I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)

10.15. Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins DQ_0, DQ_1, DQ_2 and DQ_3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

Fast Read Quad I/O with "Continuous Read Mode"

TheFastReadQuadI/Oinstructioncanfurtherreduceinstructionoverheadthroughsettingthe"Continuous Read Mode" bits (M7-0) after the input Address bits A23-A0, as shown in Figure 21. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after CS# is raised and then lowered) does not require the EBh instruction code, as shown in Figure 22. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on DQ_0 for the next instruction (8 clocks), to ensure M4= 1 and return the device to normal operation.

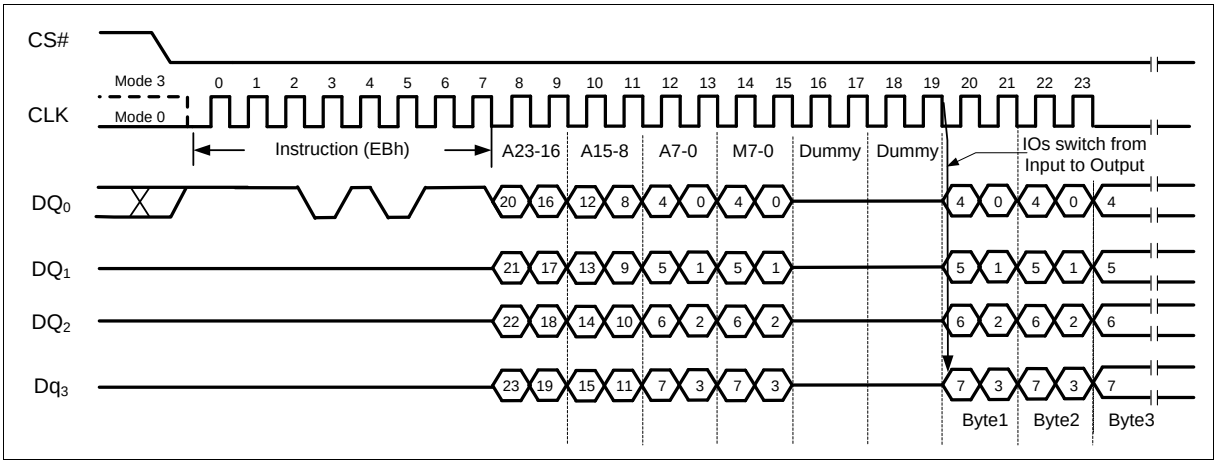


Figure 21 Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode)

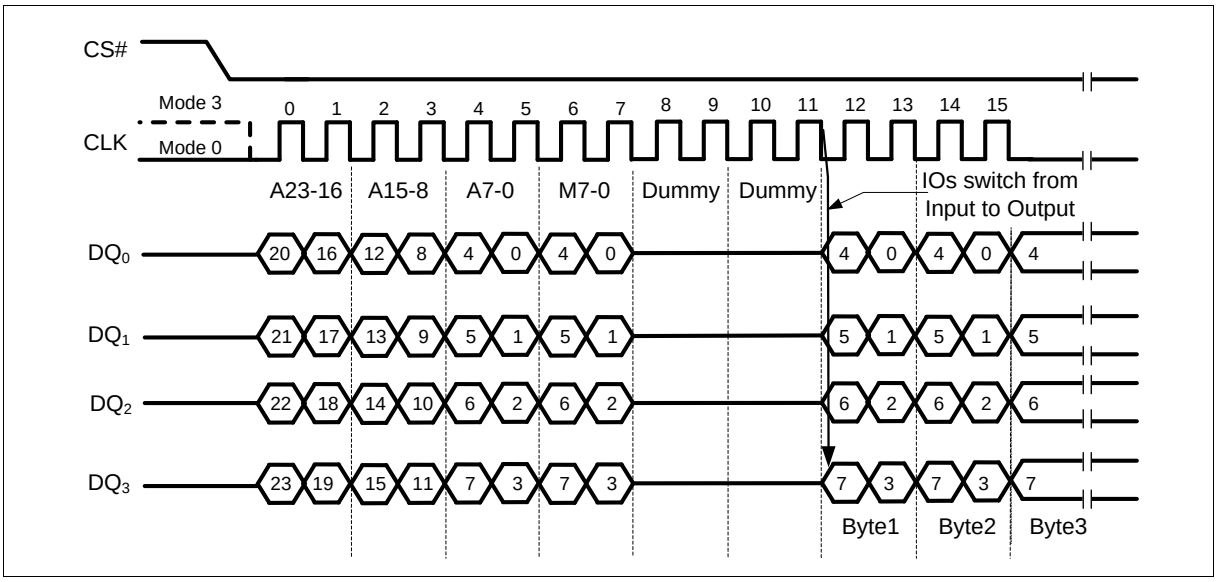


Figure 22 Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)

Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either a 8, 16, 32 or 64-byte section of a256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See "10.16Set Burst with Wrap (77h)" for detail descriptions.

10.16. Set Burst with Wrap (77h)

In Standard SPI mode, the Set Burst with Wrap (77h) instruction is used in conjunction with "Fast Read Quad I/O" instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the CS# pin low and then shifting the instruction code "77h" followed by 24 dummy bits and 8 "Wrap Bits", W7-0. The instruction sequence is shown in Figure 23. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
00	Yes	8-byte	No	N/A
01	Yes	16-byte	No	N/A
10	Yes	32-byte	No	N/A
11	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following "Fast Read Quad I/O" instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on is 1. In the case of a system Reset while W4 = 0, it is recommended that the controller issues a Set Burst with Wrap instruction to reset W4 = 1 prior to any normal Read instructions since FM25Q64AI3 does not have a hardware Reset Pin.

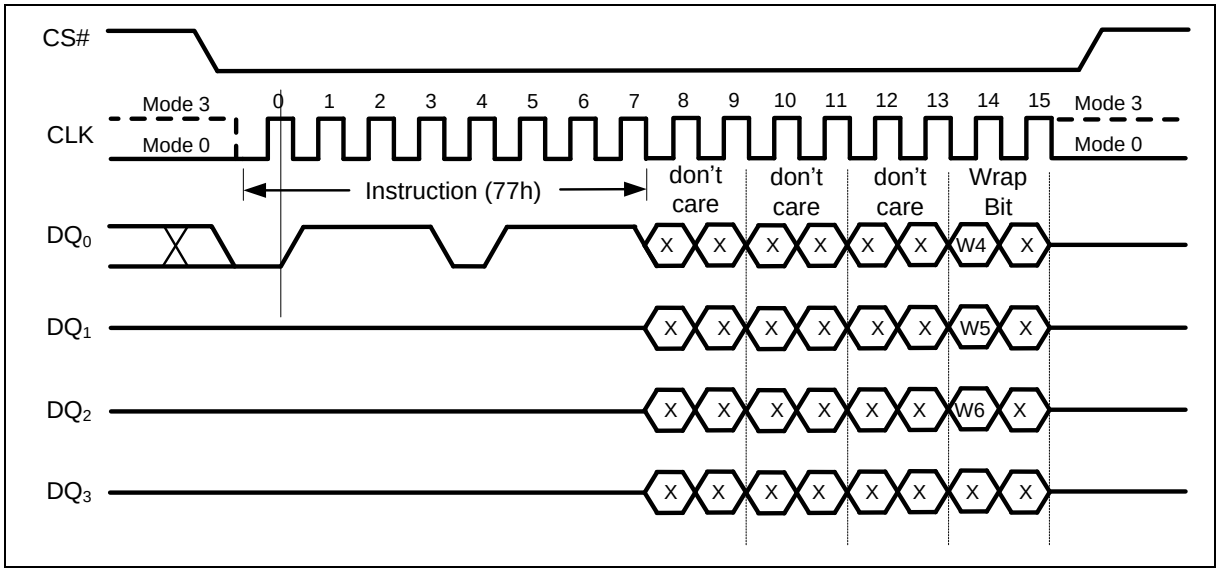


Figure 23 Set Burst with Wrap Instruction (SPI Mode)

10.17. Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “02h” followed by a 24-bit address A23-A0 and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 24.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After CS# is driven high, the self-timed Page Program instruction will commence for a time duration of t_{PP} (See “11.6AC Electrical Characteristics”). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

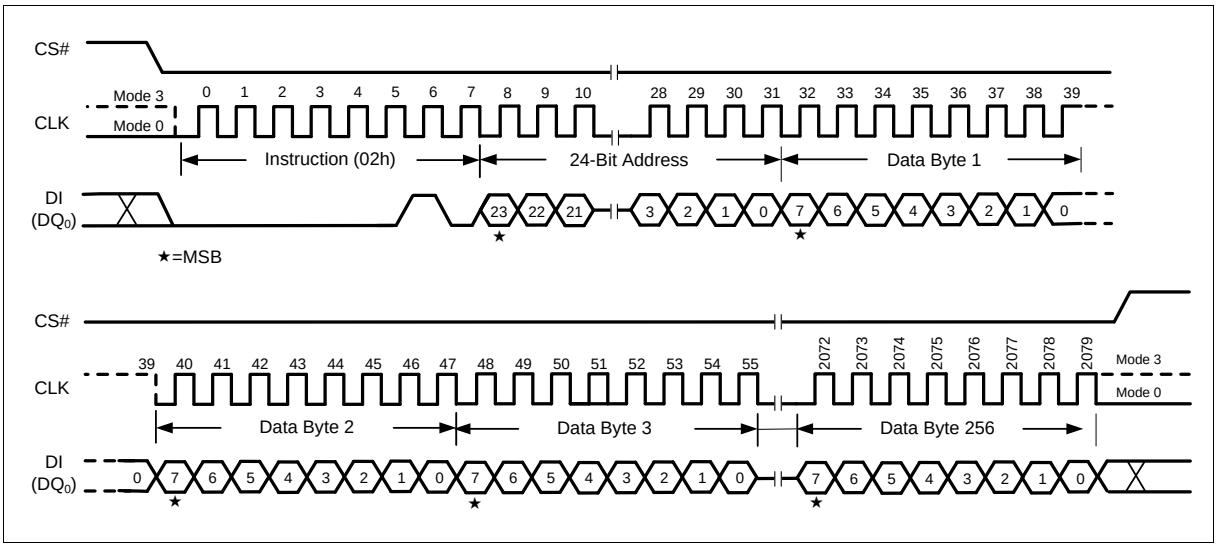


Figure 24 Page Program Instruction (SPI Mode)

10.18. Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: DQ_0, DQ_1, DQ_2, and DQ_3.The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable in Status Register-2 must be set (QE=1). A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “32h” followed by a 24-bit address A23-A0 and at least one data byte, into the DQ pins. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The QuadPage Program instruction sequence is shown in Figure 25.

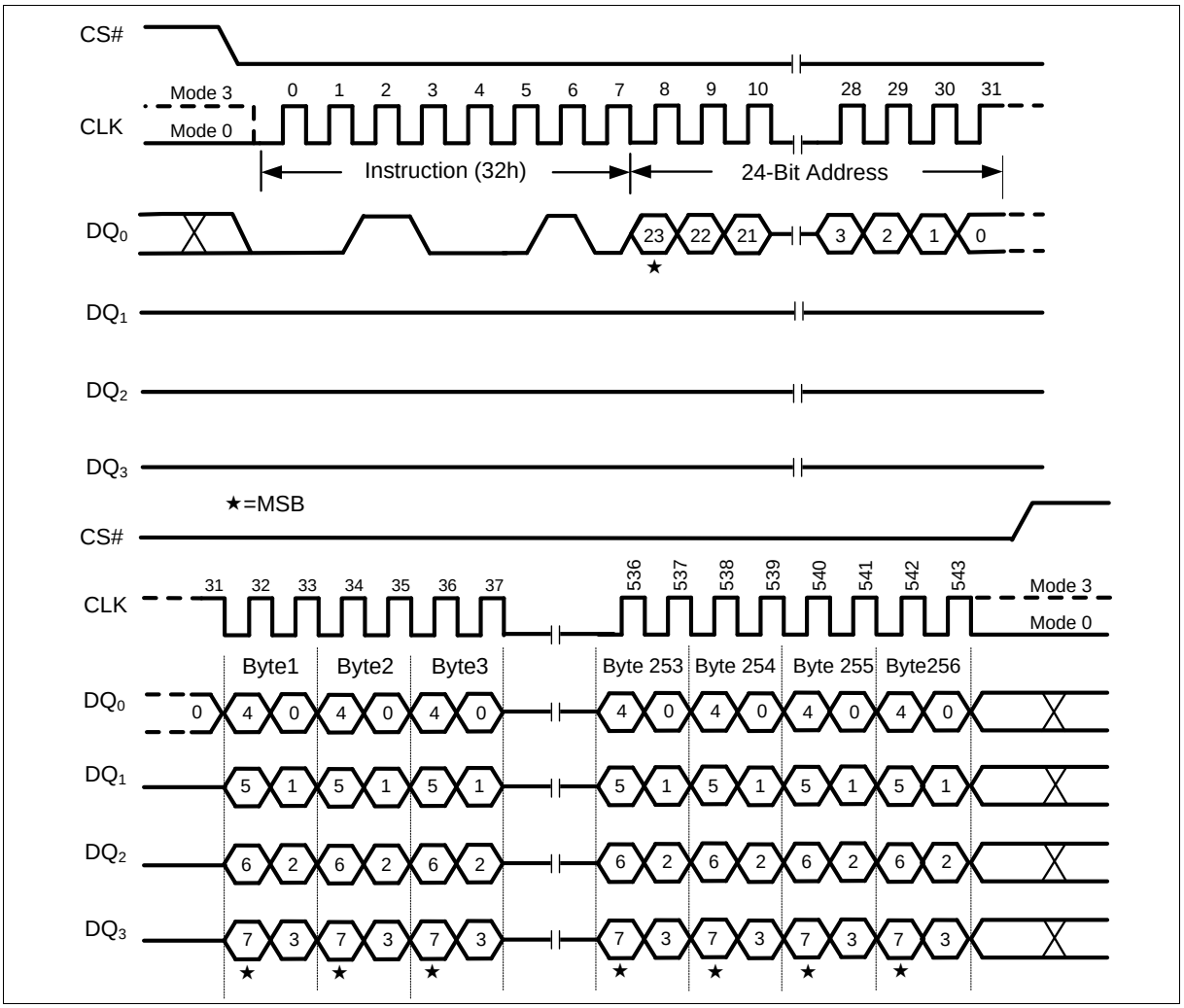


Figure 25 Quad Input Page Program Instruction (SPI Mode)

10.19. Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “20h” followed a 24-bit sector address A23-A0 (see Figure 4). The Sector Erase instruction sequence is shown in Figure 26.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After CS# is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See “11.6AC Electrical Characteristics”). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Table 3Status Register Memory Protection table).

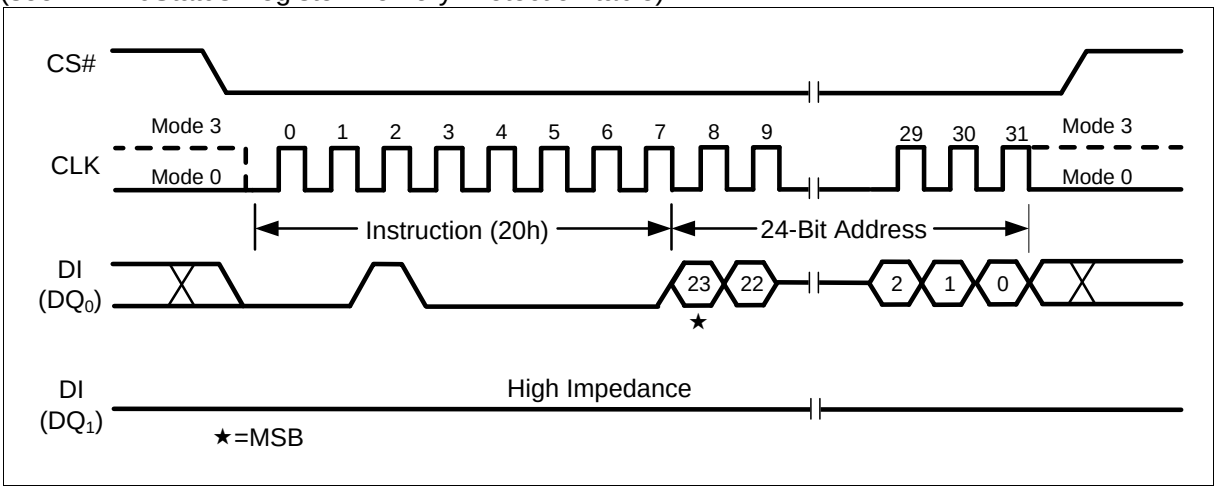


Figure 26 Sector Erase Instruction (SPI Mode)

10.20. 32KB Block Erase (BE32) (52h)

The 32KB Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instructioncode“52h” followed a 24-bit block address A23-A0. The Block Erase instruction sequence is shown in Figure 27.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE1} (See“11.6AC Electrical Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Table 3Status Register Memory Protection table).

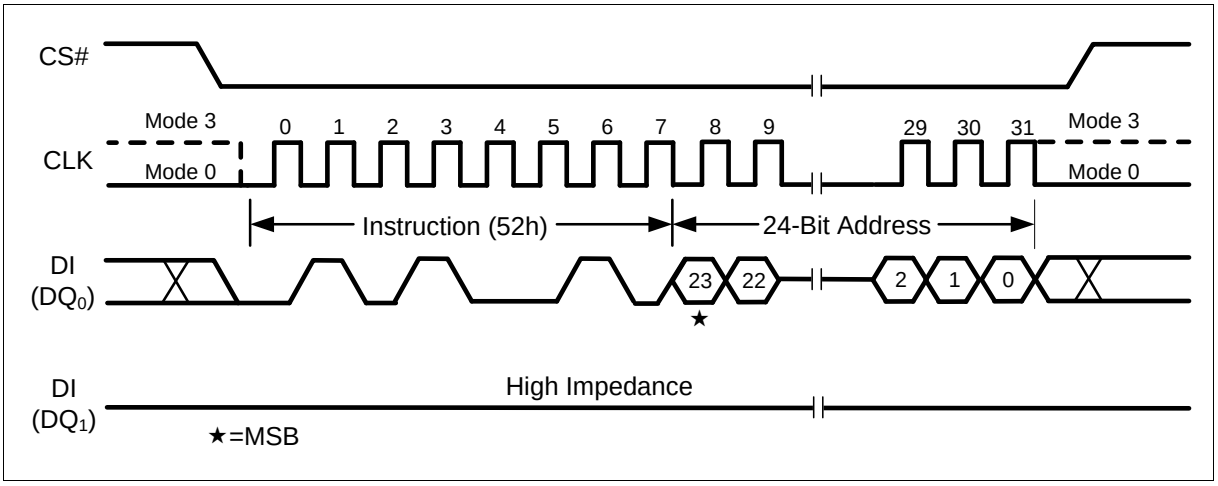


Figure 27 32KB Block Erase Instruction (SPI Mode)

10.21. 64KB Block Erase (BE) (D8h)

The 64KB Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code "D8h" followed a 24-bit block address A23-A0. The Block Erase instruction sequence is shown in Figure 28.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See 11.6AC Electrical Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Table 3 Status Register Memory Protection table).

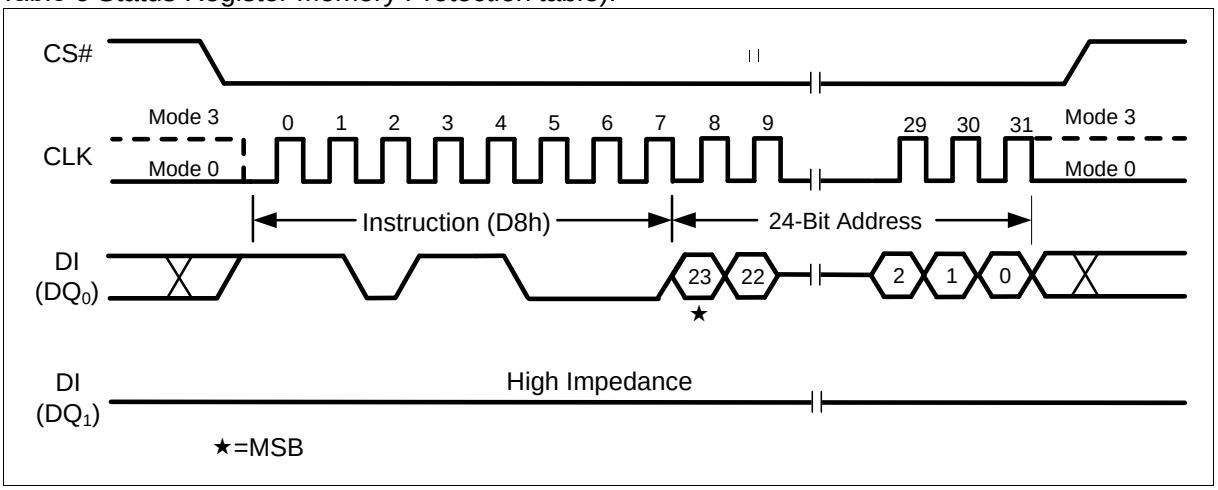


Figure 28 64KB Block Erase Instruction (SPI Mode)

10.22. Chip Erase (CE) (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 29.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After CS# is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See “11.6AC Electrical Characteristics”). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

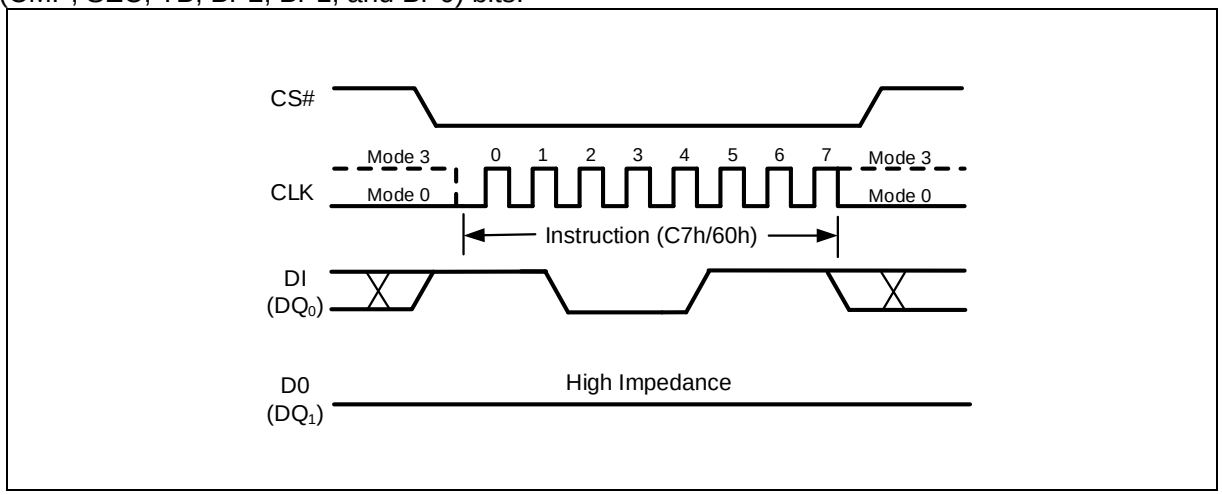


Figure 29 Chip Erase Instruction for SPI Mode

10.23. Erase / Program Suspend (75h)

The Erase/Program Suspend instruction “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 30.

The Write Status Register instruction (01h), and Erase/Program Security Registers instructions (44h, 42h), and Erase instructions (20h, 52h, D8h, C7h, 60h), and Page Program instructions (02h, 32h) are not allowed during Erase/Program Suspend. Erase/Program Suspend is valid only during the Sector/Block erase or page program operation. A maximum of time of “tsus”(See“11.6AC Electrical Characteristics”) is required to suspend the erase or program operation.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the SUS bit in the Status Register equal to 0 and the WIP bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equal to 1, or the WIP bit equals to 0, the Suspend instruction will be ignored by the device. The WIP bit in the Status Register will be cleared from 1 to 0 within “t_{SUS}” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “t_{SUS}” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

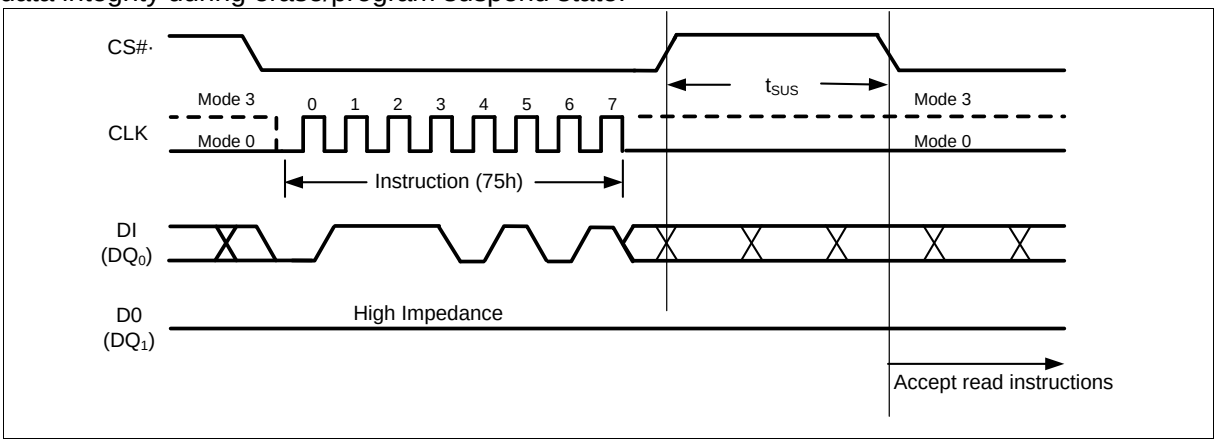


Figure 30 Erase/Program Suspend Instruction (SPI Mode)

10.24. Erase / Program Resume (7Ah)

The Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the WIP bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equal to 0 or the WIP bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 31.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “t_{SUS}” following a previous Resume instruction.

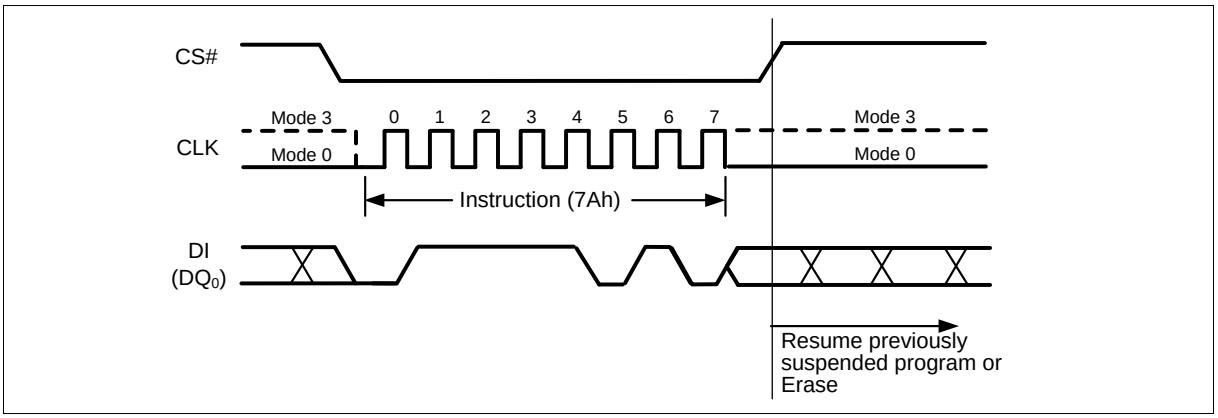


Figure 31 Erase/Program Resume Instruction (SPI Mode)

10.25. Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See I_{CC1} and I_{CC2} in“11.4DC Electrical Characteristics”). The instruction is initiated by driving the CS# pin low and shifting the instruction code “B9h” as shown in Figure 32.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After CS# is driven high, the power-down state will enter within the time duration of t_{DP} (See “11.6AC Electrical Characteristics”). While in the power-down state only the Release from Power- down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of I_{CC1}.

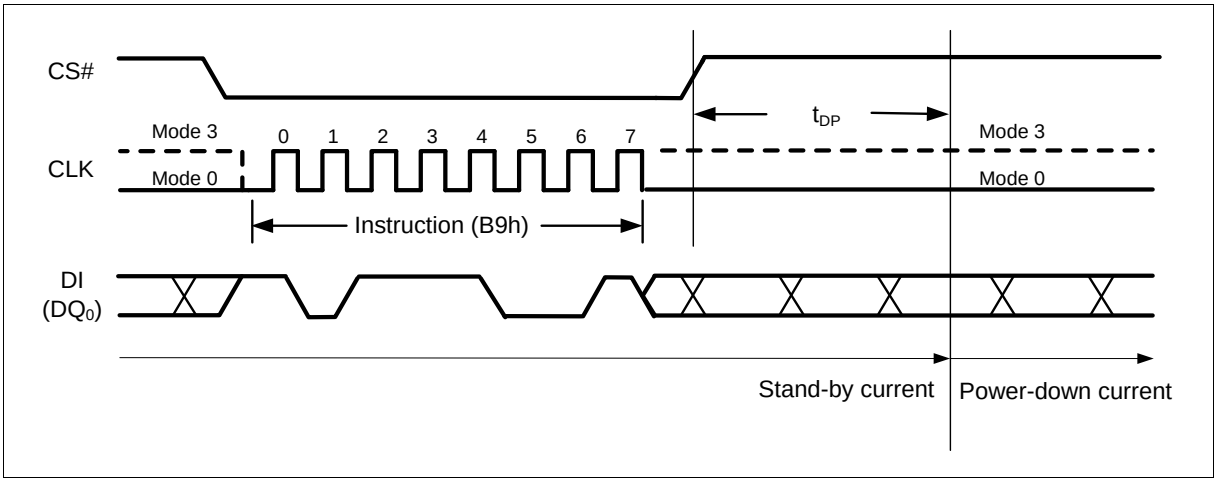


Figure 32 Deep Power-down Instruction (SPI Mode)

10.26. Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high as shown in Figure 33. Release from power-down will take the time duration of t_{RES1} (See “11.6AC Electrical Characteristics”) before the device will resume normal operation and other instructions are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 33. The Device ID value for the FM25Q64AI3 is listed in Table 4 Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in Figure 34, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See “11.6AC Electrical Characteristics”). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equals1) the instruction is ignored and will not have any effect on the current cycle.

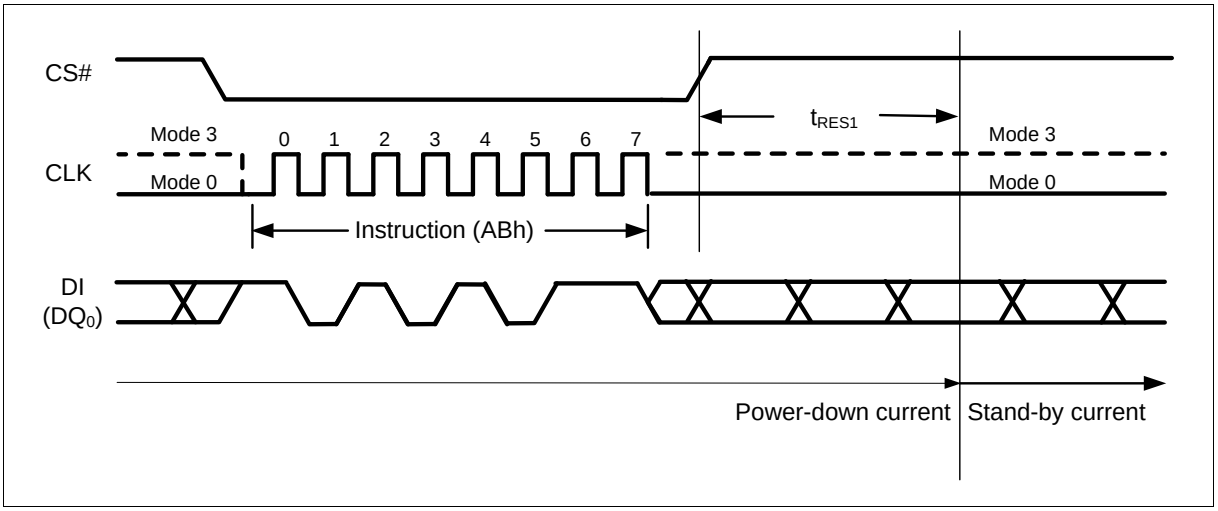


Figure 33 Release Power-down Instruction (SPI Mode)

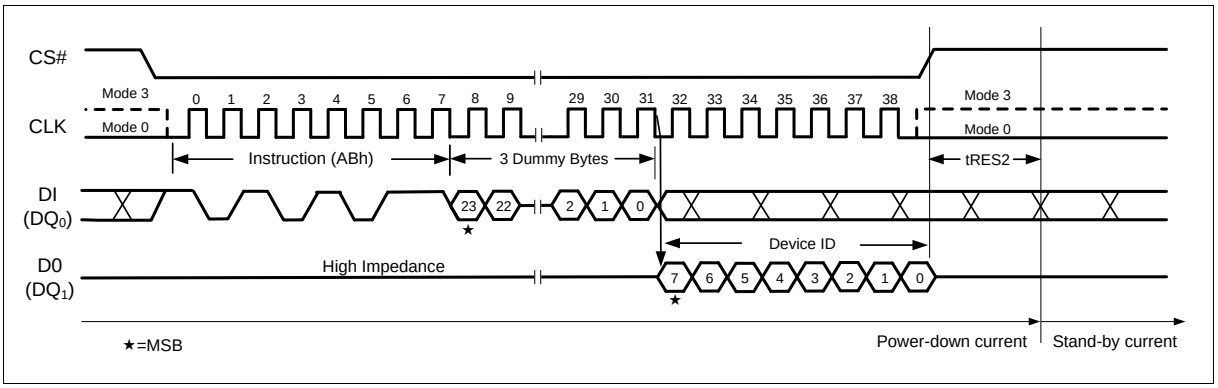


Figure 34 Release Power-down / Device ID Instruction (SPI Mode)

10.27. Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “90h” followed by a 24-bit address A23-A0 of 000000h. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 35. The Device ID value for the FM25Q64AI3 is listed in Table 4 Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

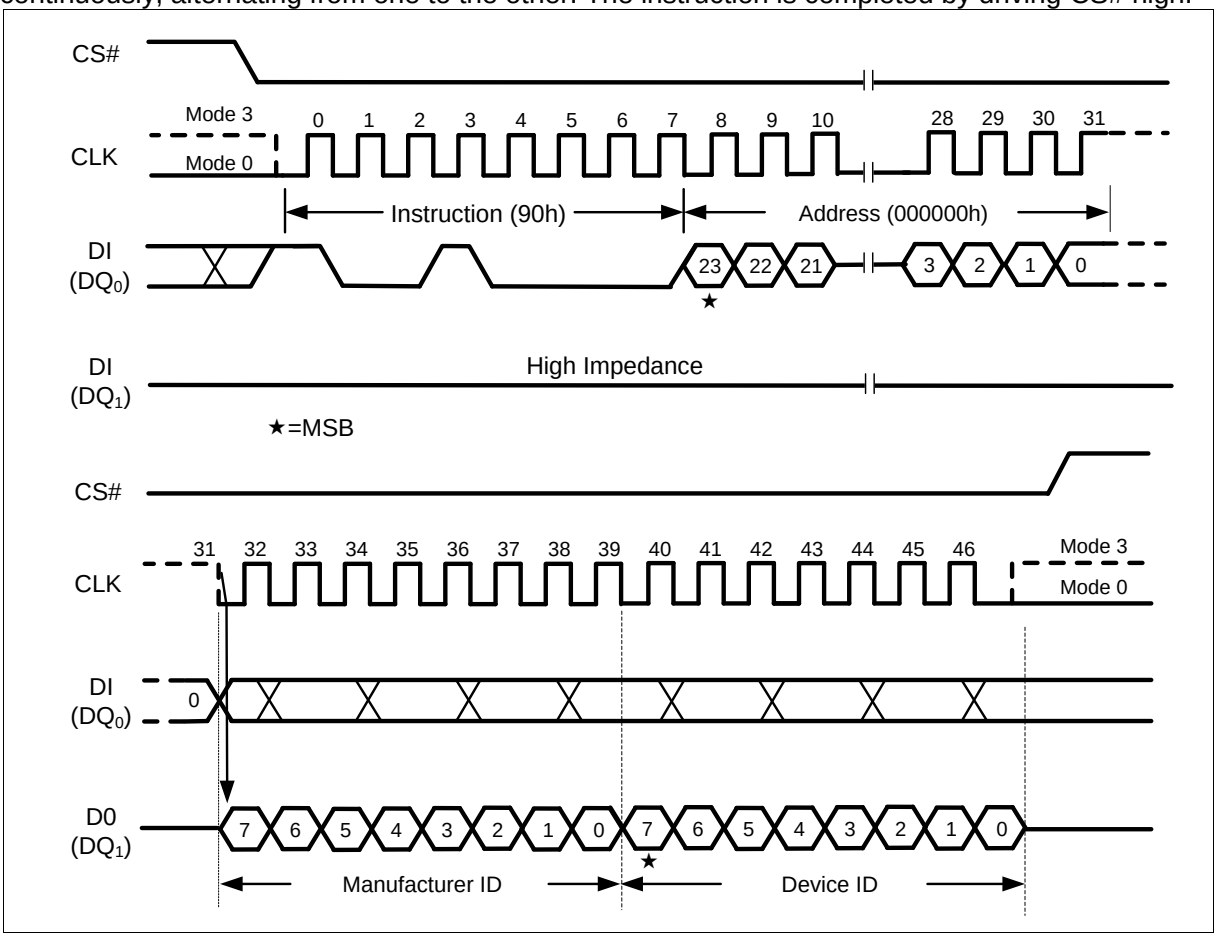


Figure 35 Read Manufacturer / Device ID Instruction (SPI Mode)

10.28. Read Manufacturer/ Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "92h" followed by a24-bit address A23-A0 of 000000h, 8-bit Continuous Read Mode Bits, with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 36. The Device ID value for the FM25Q64AI3 is listed in Table 4 Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

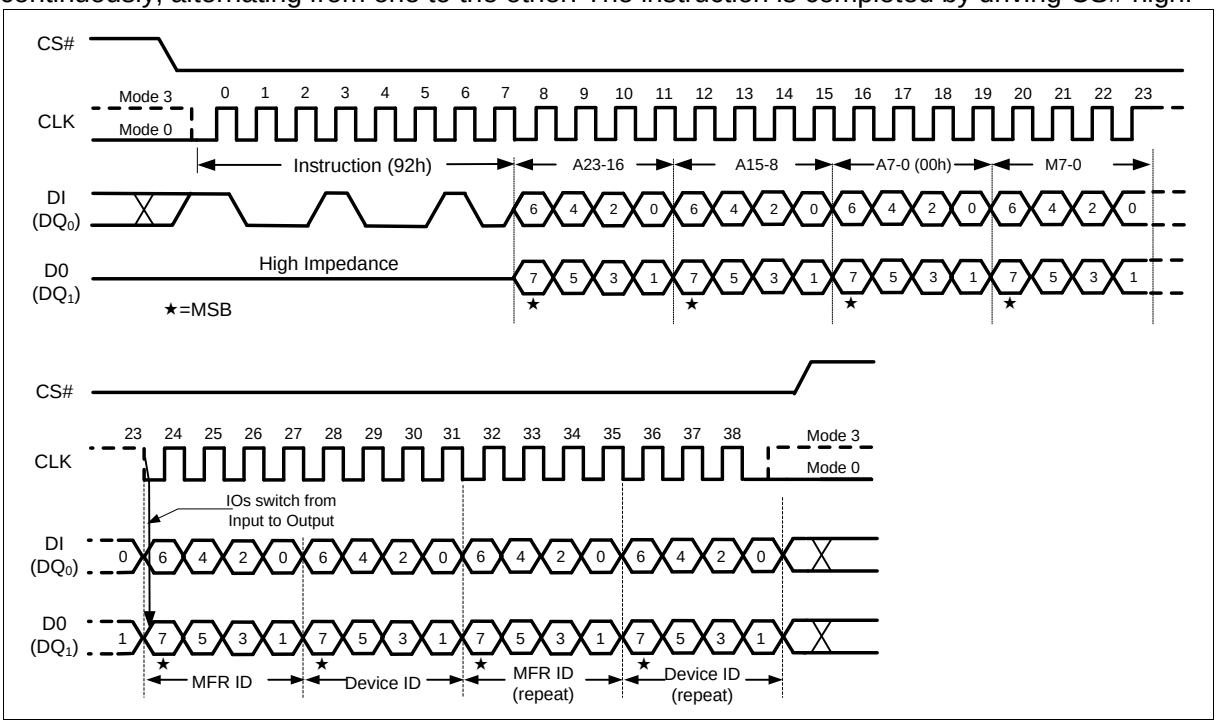


Figure 36 Read Manufacturer / Device ID Dual I/O Instruction (SPI Mode)

Note:
The "Continuous Read Mode" bits M7-M0 must be set to Fxh to be compatible with Fast Read Dual I/O instruction.

10.29. Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "94h" followed by a 24-bit address A23-A0 of 000000h, 8-bit Continuous Read Mode Bits and then four clock dummy cycles, with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 37. The Device ID value for the FM25Q64AI3 is listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

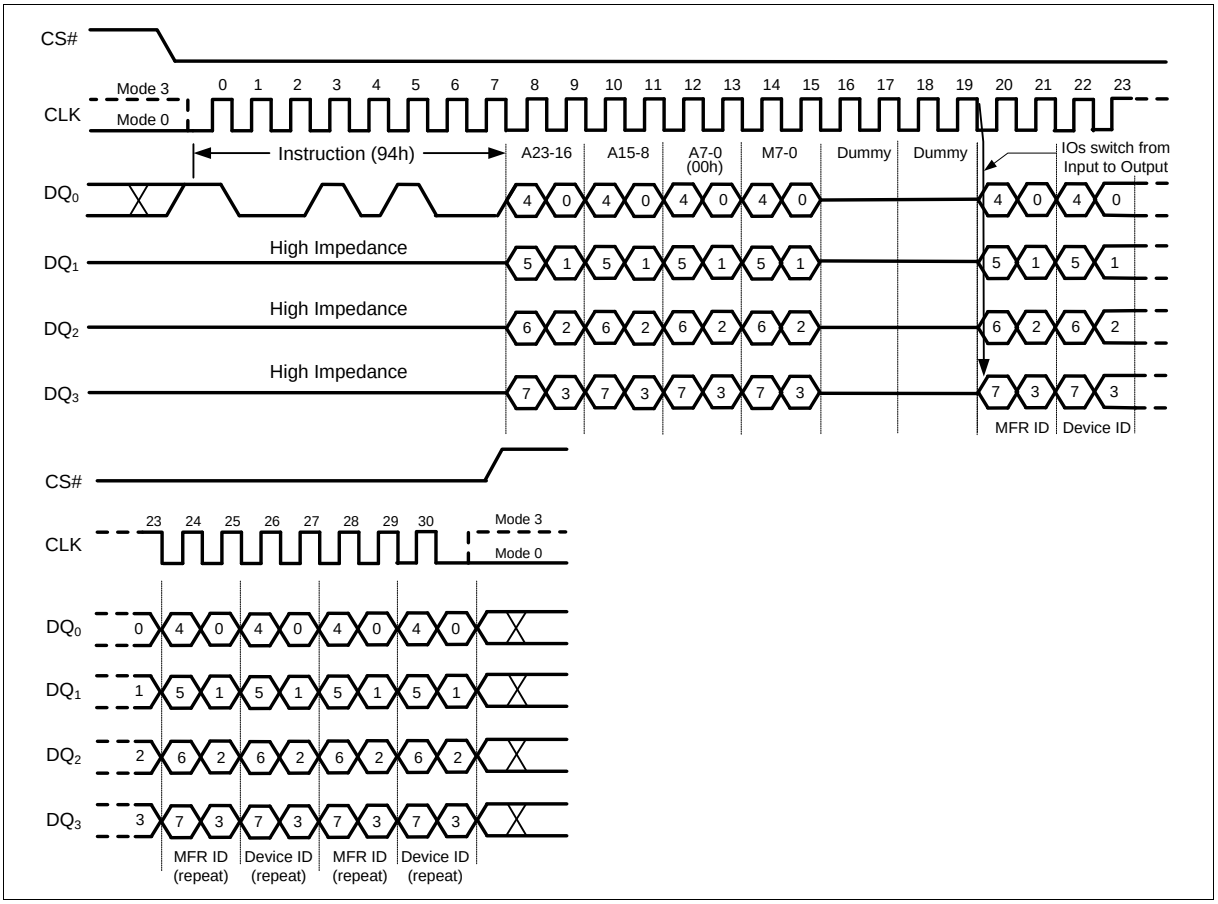


Figure 37 Read Manufacturer / Device ID Quad I/O Instruction (SPI Mode)

Note:
The "Continuous Read Mode" bits M7-M0 must be set to Fxh to be compatible with Fast Read Quad I/O instruction.

10.30. Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each FM25Q64AI3 device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the CS# pin low and shifting the instruction code “4Bh” followed by a four bytes of dummy clocks. After which, the 64- bit ID is shifted out on the falling edge of CLK as shown in Figure 38.

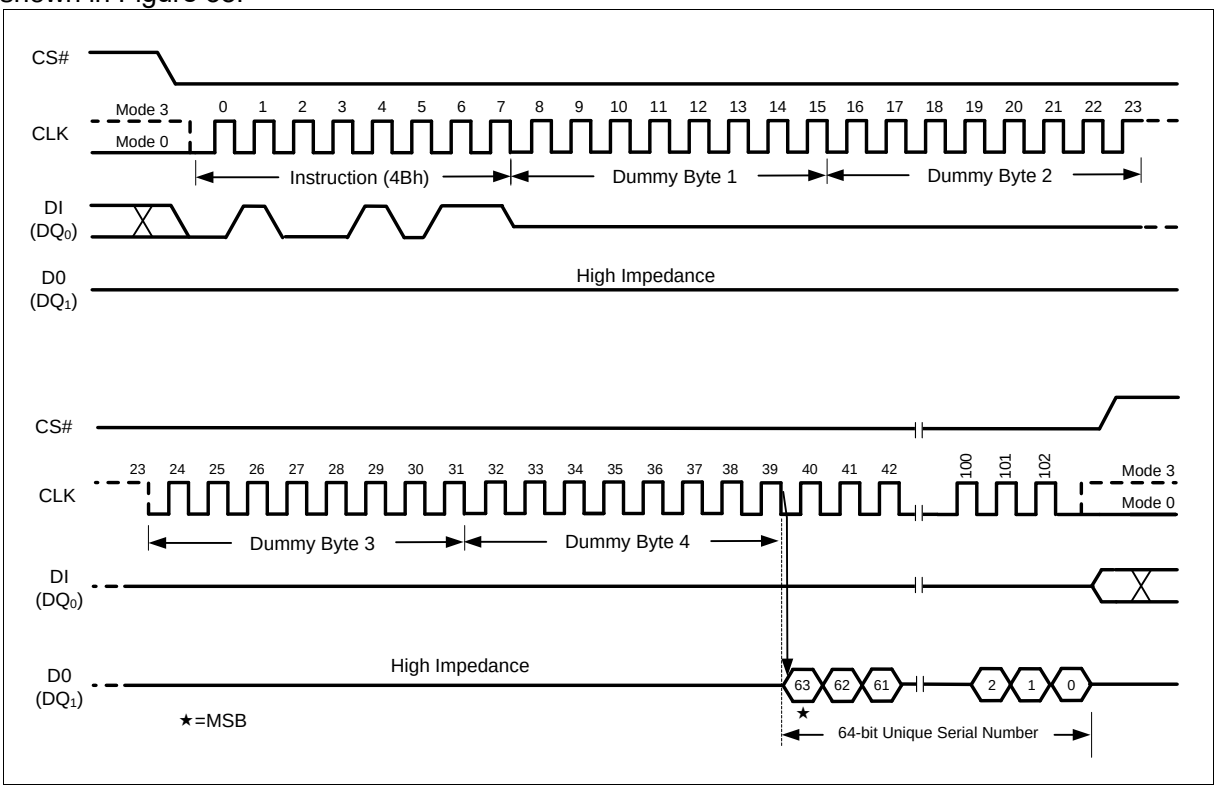


Figure 38 Read Unique ID Number Instruction (SPI Mode)

10.31. Read JEDEC ID (9Fh)

For compatibility reasons, the FM25Q64AI3 provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories. The instruction is initiated by driving the CS# pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity ID7-ID0 are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 39. For memory type and capacity values refer to Table 4 Manufacturer and Device Identification table.

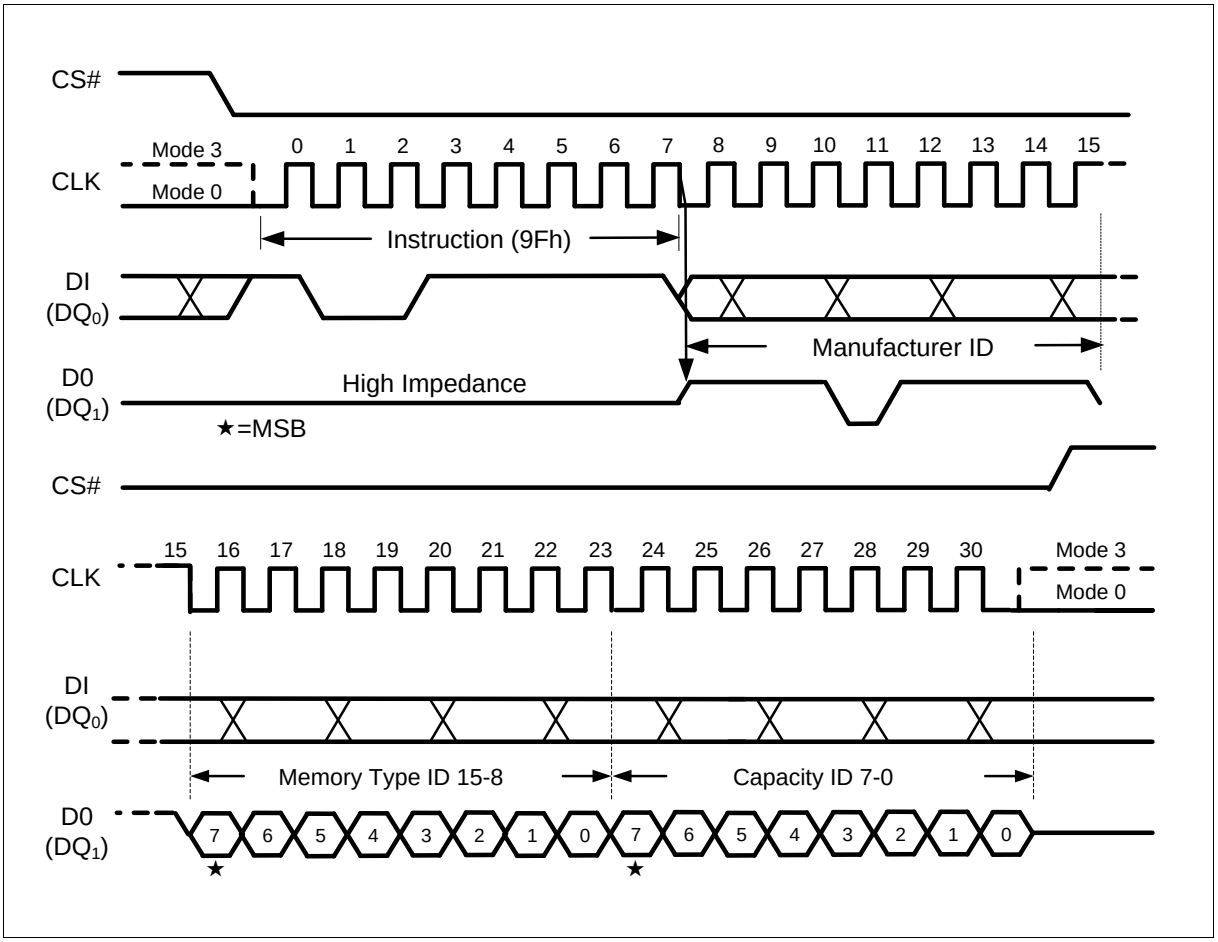


Figure 39 Read JEDEC ID Instruction (SPI Mode)

10.32. Read SFDP Register(5Ah)

The FM25Q64AI3 features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The concept of SFDP is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216B.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code "5Ah" followed by a 24-bit address (A23-A0)(1) into the DI pin. Eight "dummy" clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 40.

For SFDP register values and descriptions, refer to the following SFDP Definition table.

Note: 1. A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

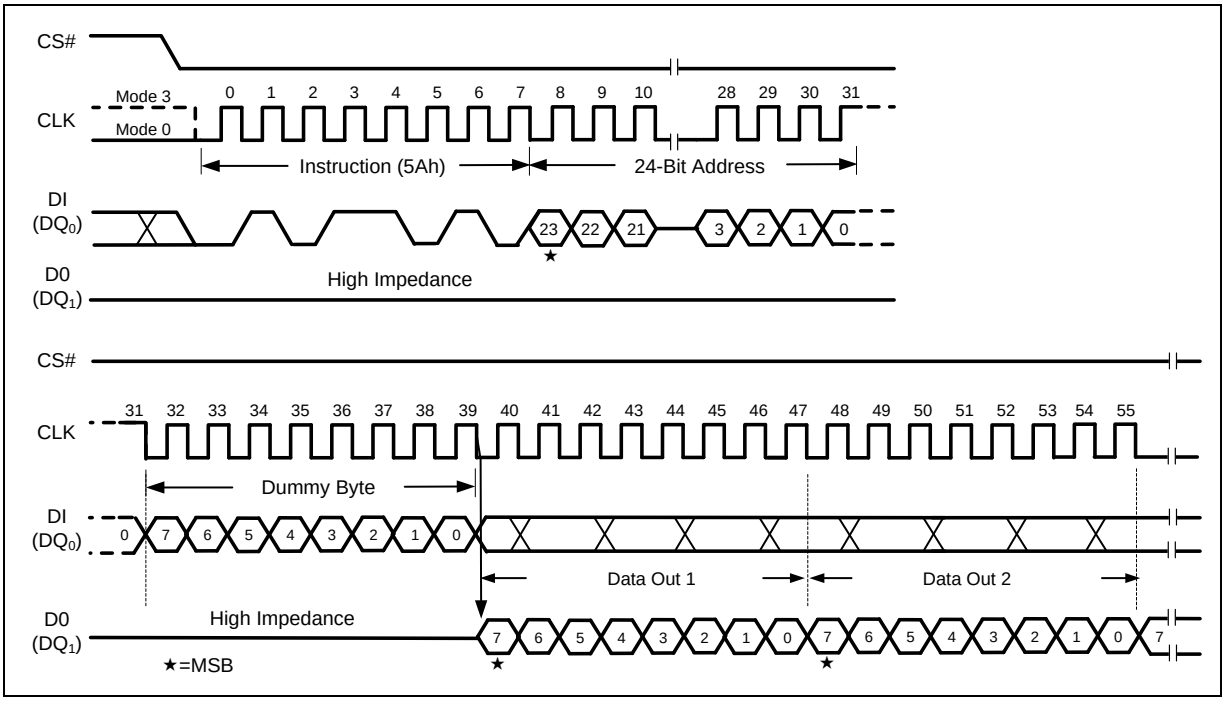


Figure 40 Read SFDP Register Instruction

Serial Flash Discoverable Parameter Definition Table

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
00h	53h	SFDP Signature	SFDP Signature = 50444653h
01h	46h	SFDP Signature	
02h	44h	SFDP Signature	
03h	50h	SFDP Signature	
04h	06h	SFDP Minor Revision Number	JESD216B
05h	01h	SFDP Major Revision Number	
06h	00h	Number of Parameter Headers (NPH)	1 Parameter Header
07h	FFh	Reserved	
08h	00h	PID(3)(0): ID Number	00h=JEDEC specified

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
09h	06h	PID(0): Parameter Table Minor Revision Number	JESD216B
0Ah	01h	PID(0): Parameter Table Major Revision Number	
0Bh	10h	PID(0): Parameter Table Length	16Dwords(2)
0Ch	80h	PID(0): Parameter Table Pointer (PTP) (A7-A0)	PID(0) Pointer = 000080h
0Dh	00h	PID(0): Parameter Table Pointer (PTP) (A15-A8)	
0Eh	00h	PID(0): Parameter Table Pointer (PTP) (A23-A16)	
0Fh	FFh	Reserved	
10h	FFh	Reserved	
...(1)	FFh	Reserved	
7Fh	FFh	Reserved	
80h	E5h	Bit[1:0]=01 Supports 4KB Bit[2]=1 Page Programmable Bit[4:3]=00 Non-volatile Status Register Bit[7:5]=111 Reserved	
81h	20h	4K-Byte Erase Opcode	
82h	F1h	Bit[16] =1 Supports (1-1-2) Fast Read Bit[18:17]=00 3-Byte/24-Bit Only Addressing Bit[19] =0 Not support Dual Transfer Rate Bit[20] =1 Supports (1-2-2) Fast Read Bit[21] =1 Supports (1-4-4) Fast Read Bit[22] =1 Supports (1-1-4) Fast Read Bit[23] =1 Reserved	
83h	FFh	Reserved	
84h	FFh	Flash Size in Bits	64 Mega Bits = 03FFFFFFh
85h	FFh	Flash Size in Bits	
86h	FFh	Flash Size in Bits	
87h	03h	Flash Size in Bits	
88h	44h	Bit[4:0]=00100 16 Dummy Bits are needed Bit[7:5]=010 8 Mode Bits are needed	Fast Read Quad I/O Setting
89h	EBh	Quad Input Quad Output Fast Read Opcode	
8Ah	08h	Bit[7:5]=000 No Mode Bits are needed Bit[4:0]=01000 8 Dummy Bits are needed	Fast Read Quad Output Setting
8Bh	6Bh	Single Input Quad Output Fast Read Opcode	
8Ch	08h	Bit[4:0]=01000 8 Dummy Bits are needed Bit[7:5]=000 No Mode Bits are needed	Fast Read Dual Output Setting
8Dh	3Bh	Single Input Dual Output Fast Read Opcode	
8Eh	80h	Bit[20:16]=00000 No Dummy bits are needed Bit[23:21]=100 8 Mode bits are needed	Fast Read Dual I/O Setting
8Fh	BBh	Dual Input Dual Output Fast Read Opcode	
90h	EEh	Bit[0]=0 Not support (2-2-2) Fast Read Bit[3:1]=111 Reserved Bit[4]=0 not support (4-4-4) Fast Bit[7:5]=111 Reserved	
91h	FFh	Reserved	
92h	FFh	Reserved	
93h	FFh	Reserved	
94h	FFh	Reserved	
95h	FFh	Reserved	
96h	00h	No Mode Bits or Dummy Bits for (2-2-2) Fast Read	
97h	00h	Not support (2-2-2) Fast Read	
98h	FFh	Reserved	

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
99h	FFh	Reserved	
9Ah	00h	No Mode Bits or Dummy Bits for (4-4-4) Fast Read	
9Bh	00h	Not support (4-4-4) Fast Read	
9Ch	0Ch	Sector Type 1 Size (4KB)	Sector Erase Type &Opcode
9Dh	20h	Sector Type 1 Opcode	
9Eh	0Fh	Sector Type 2 Size (32KB)	
9Fh	52h	Sector Type 2 Opcode	
A0h	10h	Sector Type 3 Size (64KB)	Sector Erase Type &Opcode
A1h	D8h	Sector Type 3 Opcode	
A2h	00h	Sector Type 4 Size (256KB) – Not supported	
A3h	00h	Sector Type 4 Opcode – Not supported	
A4h	33h	Bit[3:0]=0011 Multiplier from typical erase time to maximum erase time Bit[10:4]=0100011 Erase type1 erase typical time= 30ms/64ms Bit[17:11]=0101100 Erase type2 erase typical time= 150ms/208ms Bit[24:18]=0110010 Erase type3 erase typical time= 200ms/304ms Bit[31:25]=1111111 Erase type4 not exist	Typical Erase Times and Multiplier Used to Derive Max Erase Times
A5h	62h		
A6h	C9h		
A7h	FEh		
A8h	82h	Bit[3:0]=0010 Multiplier from typical time to maximum time for Page or Byte program Bit[7:4]=1000 Page size= 256 Bytes	Chip Erase Typical Time, Byte Program and Page Program Typical Times, Page Size
A9h	E9h	Bit[13:8]=101001 Page program time= 600us/ 640us Bit[18:14]=10111 First Byte program=60us/64us Bit[23:19]=00000 Reserved Bit[30:24]=1000110 Chip erase typical time= 25s/ 28s Bit[31]=0 Reserved	
AAh	05h		
ABh	46h		
ACh	88h	Bit[3:0]=1000 Prohibited Operations During Program Suspend Bit[7:4]=1000 Prohibited Operations During Erase Suspend	Erase/Program Suspend/Resume Support, Intervals, Latency, Keep Out Areas Size
ADh	A0h	Bit[8]=0 Reserved Bit[12:9]=0000 Program Resume to Suspend Interval Time = 30us/ 64us	
AEh	07h	Bit[19:13]=0111101 Suspend in-progress Program Max Latency Time= 30us/30us Bit[23:20]=0000 Erase Resume to Suspend Interval Time = 30us/ 64us	
AFh	3Dh	Bit[30:24]=0111101 Suspend in-progress Erase Max Latency Time= 30us/30us Bit[31]=0 Suspend/Resume Supported	
B0h	7Ah	Program Resume Instruction	Program/Erase Suspend/Resume Instructions
B1h	75h	Program Suspend Instruction	
B2h	7Ah	Resume Instruction	
B3h	75h	Suspend Instruction	
B4h	04h	Bit[1:0]=00 Reserved Bit[7:2]=000001 Use of legacy polling is supported by reading the Status Register with 05h instruction and checking WIP bit[0] (0=ready; 1=busy)	Deep Power down and Status Register Polling Device Busy

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
B5h	A2h	Bit[14:8]=0100010 Exit Deep Power down to next operation delay =3us/3us Bit[22:15]=ABh=10101011 Exit Deep Power down Instruction Bit[30:23]=B9h=10111001 Enter Deep Power down Instruction Bit[31]=0 Support deep power down	
B6h	D5h		
B7h	5Ch		
B8h	00h	Bit[3:0]=0000 Not support 4-4-4 mode Bit[7:4]=0000 Not support 4-4-4 mode	Hold and WP Disable Function, Quad Enable Requirements, 4-4-4 Mode Enable/Disable Sequences, 0-4-4 Entry/Exit Methods and Support
B9h	06h	Bit[8]=0 Not support 4-4-4 mode Bit[9]=1 Support 0-4-4 Bit[15:10]=000001 M<7:0>=00H, 0-4-4 Mode Exit Method	
BAh	44h	Bit[19:16]=0100 M<7:0>=AXH, 0-4-4 Mode Entry Method Bit[22:20]=100 QE is in status register 2, bit 1 Bit[23]=0 Not support HOLD or RESET Disable	
BBh	00h	Reserved	
BCh	08h	Bit[6:0]=0001000 Volatile or Non-Volatile Register and Write Enable Instruction for Status Register 1 Bit[7]=0 Reserved	32-bit Address Entry/Exit Methods and Support, Soft Reset and Rescue Sequences, Volatile and Nonvolatile Status Register Support
BDh	10h	Bit[13:8]=010000 Soft Reset and Rescue Sequence Support(66H-99H) Bit[23:14]=1000000000 Reserved	
BEh	80h		
BFh	80h	Bit[31:24]=10000000 Reserved	
...(1)	FFh	Reserved	
FFh	FFh	Reserved	

Notes:
1. Data stored in Byte Address 10h to 7Fh&C0h toFFh areReserved, thevalue isFFh.
2. 1Dword=4 Bytes
3. PID(x)= Parameter IdentificationTable (x)

10.33. Erase Security Sectors (44h)

The FM25Q64AI3 offers one 1024-byte Security Sector. The Security Sector may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Sector instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Sector Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “44h” followed by a 24-bit address A23-A0 to erase Security Sectors.

A23-16	A15-10	A9-0
00h	000000	Don’t Care

The Erase Security Sector instruction sequence is shown in Figure 41. The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After CS# is driven high, the self-timed Erase Security Sector operation will commence for a time duration of t_{SE} (See “11.6AC Electrical Characteristics”). While the Erase Security Sector cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Sector cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Sector Lock Bit (LB) in the Status Register-2 can be used to OTP protect the Security Sectors. Once the LB bit is set to 1, the Security Sector will be permanently locked, Erase Security Sector instruction will be ignored.

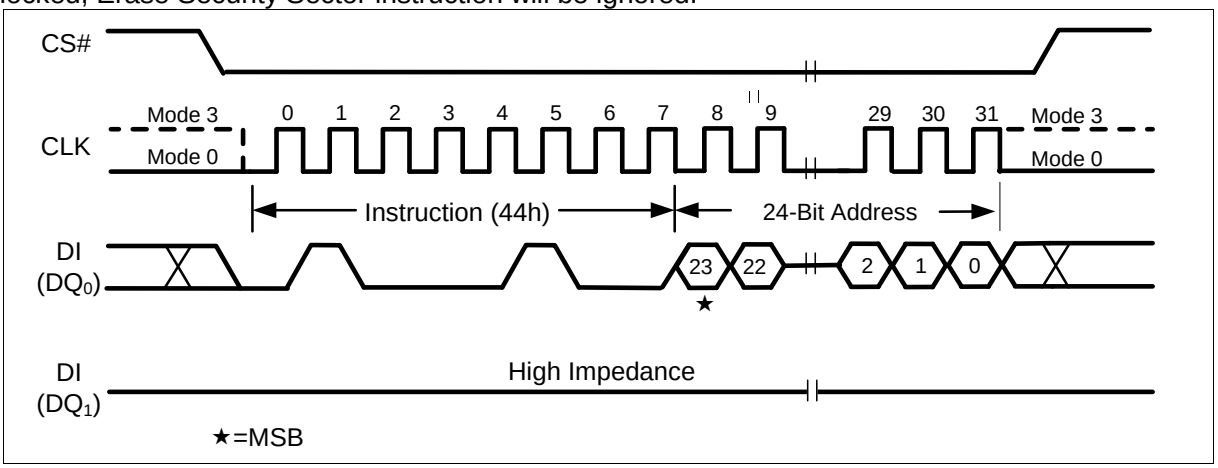


Figure 41 Erase Security Sectors Instruction (SPI Mode)

10.34. Program Security Sectors (42h)

The Program Security Sector instruction is similar to the Page Program instruction. It allows from one byte to256bytes of Security Sectordatato be programmed at previously erased(FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Sector Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “42h” followed by a 24-bit address A23-A0 and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device.

A23-16	A15-10	A9-8	A7-0
00h	0 0 0 0	0 0 0 1 1 0 1 1	Byte Address

The Program Security Sector instruction sequence is shown in Figure 42. The Security Sector Lock Bit (LB) in the Status Register-2 can be used to OTP protect the Security Sectors. Once a lock bit is set to 1, the Security Sector will be permanently locked, Program Security Sector instruction will be ignored.

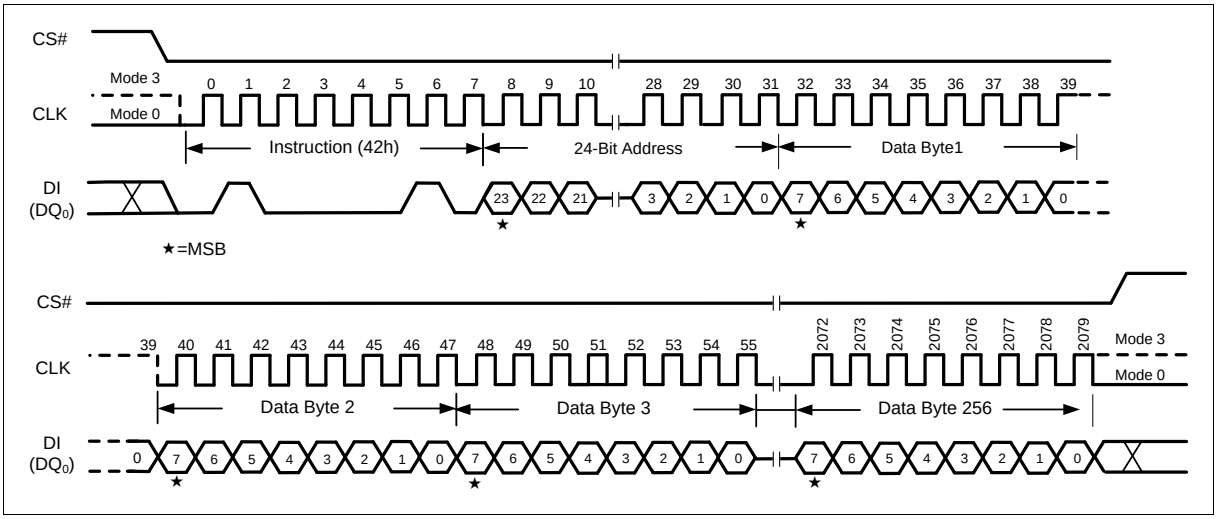


Figure 42 Program Security Sectors Instruction (SPI Mode)

10.35. Read Security Sectors (48h)

The Read Security Sector instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the twoSecurity Sectors. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “48h”followed by a 24-bit address A23-A0 and eight “dummy” clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte 3FFh), it will be reset to 00h, the first byte of the register, and continue to increment. The instruction is completed by driving CS# high. The Read Security Sector instruction sequence is shown in Figure 43. If a Read Security Sector instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effect on the current cycle. The Read Security Sector instruction allows clock rates from D.C. to a maximum of FR (see “11.6AC Electrical Characteristics”).

A23-16	A15-10	A9-8	A7-0
00h	0 0 0 0	0 0 0 1 1 0 1 1	Byte Address

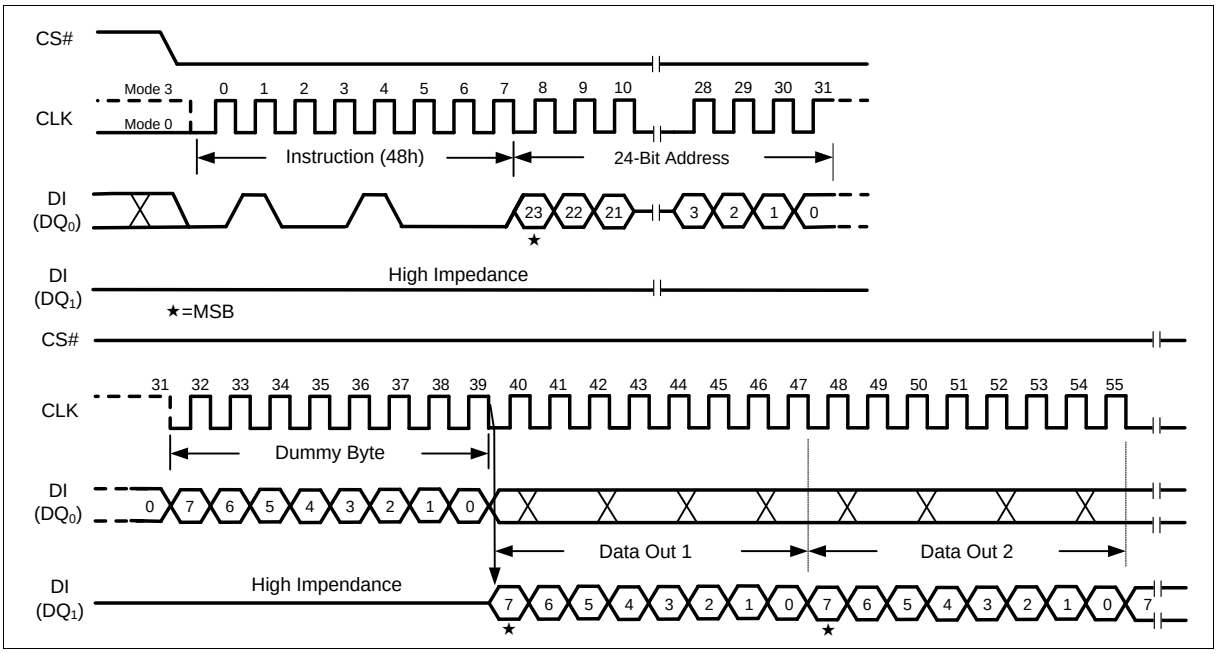


Figure 43 Read Security Sectors Instruction (SPI Mode)

10.36. Enable Reset (66h) and Reset (99h)

Because of the small package and the limitation on the number of pins, the FM25Q64AI3 provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Read parameter setting P7-P0, Continuous Read Mode bit setting M7-M0 and Wrap Bit setting W6-W4.

“Enable Reset (66h)” and “Reset (99h)” instructions can be issued in SPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than “Reset (99h)” after the “Enable Reset (66h)” command will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately t_{RST}=30μs to reset. During this period, no command will be accepted.

Data corruptionmay happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence isaccepted by the device. It is recommended to check the WIP bit and the SUS bit in Status Register before issuing theReset command sequence.

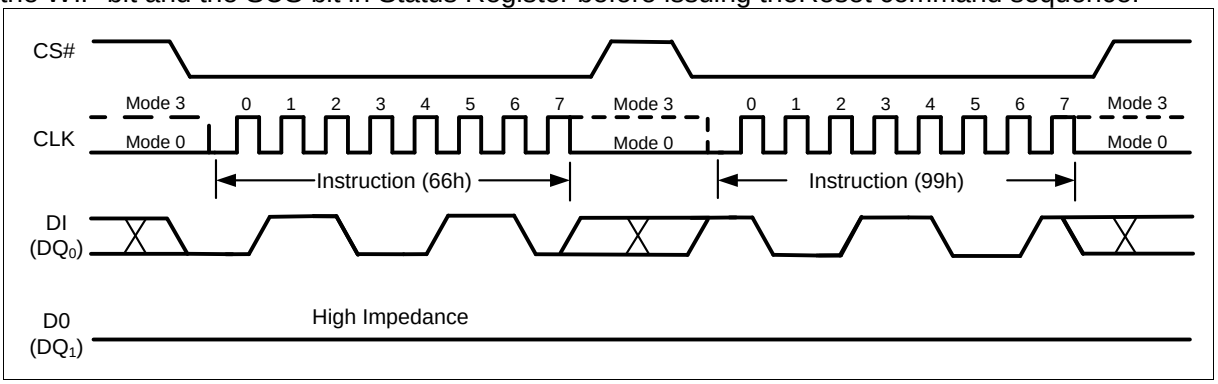


Figure 44 Enable Reset and Reset Instruction Sequence (SPI Mode)

11. Electrical Characteristics

11.1. Absolute Maximum Ratings

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on I/O Pinwith Respect to Ground	-0.5V to V_{CC}+0.4V
Transient Input/Output Voltage(note: overshoot <20ns)	-2.0V to V_{CC} +2.0V
V_{CC}	-0.5V to 4.0V

*NOTICE: Stresses beyond those listed under"Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 45 Maximum Negative Overshoot Waveform

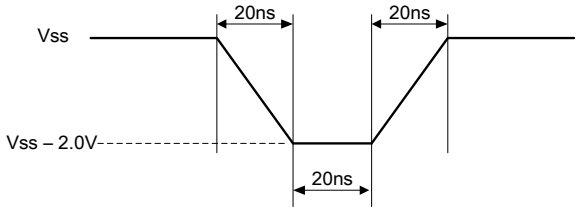
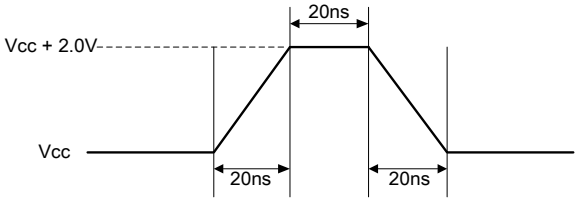


Figure 46Maximum Positive Overshoot Waveform



11.2. Pin Capacitance

PARAMETER	SYMBOL	CONDITIONS	Max	Units
Input Capacitance	C_{IN}(1)	V_{IN} = 0V, f = 5 MHz	6	pF
Output Capacitance	C_{OUT}(1)	V_{OUT} = 0V, f = 5 MHz	8	pF

Note: 1. This parameter is characterized and is not 100% tested.

11.3. Power-up Timing

Applicable over recommended operating range from: T_A= -40°C to 85°C, V_{CC} = 2.7V to 3.6V,(unless otherwise noted).

SYMBOL	PARAMETER		SPEC		UNIT
			MIN	MAX	
t_{VSL}	VCC (min) to CS# Low		100		µs
V_{WI}	Write Inhibit Threshold Voltage		1	2.2	V
V_{PWD}	VCC voltage needed to below V_{PWD} for ensuring initialization will occur	Deep Power Down		0.4	V
		others		0.9	V
t_{PWD}	The minimum duration for ensuring initialization will occur		1		ms

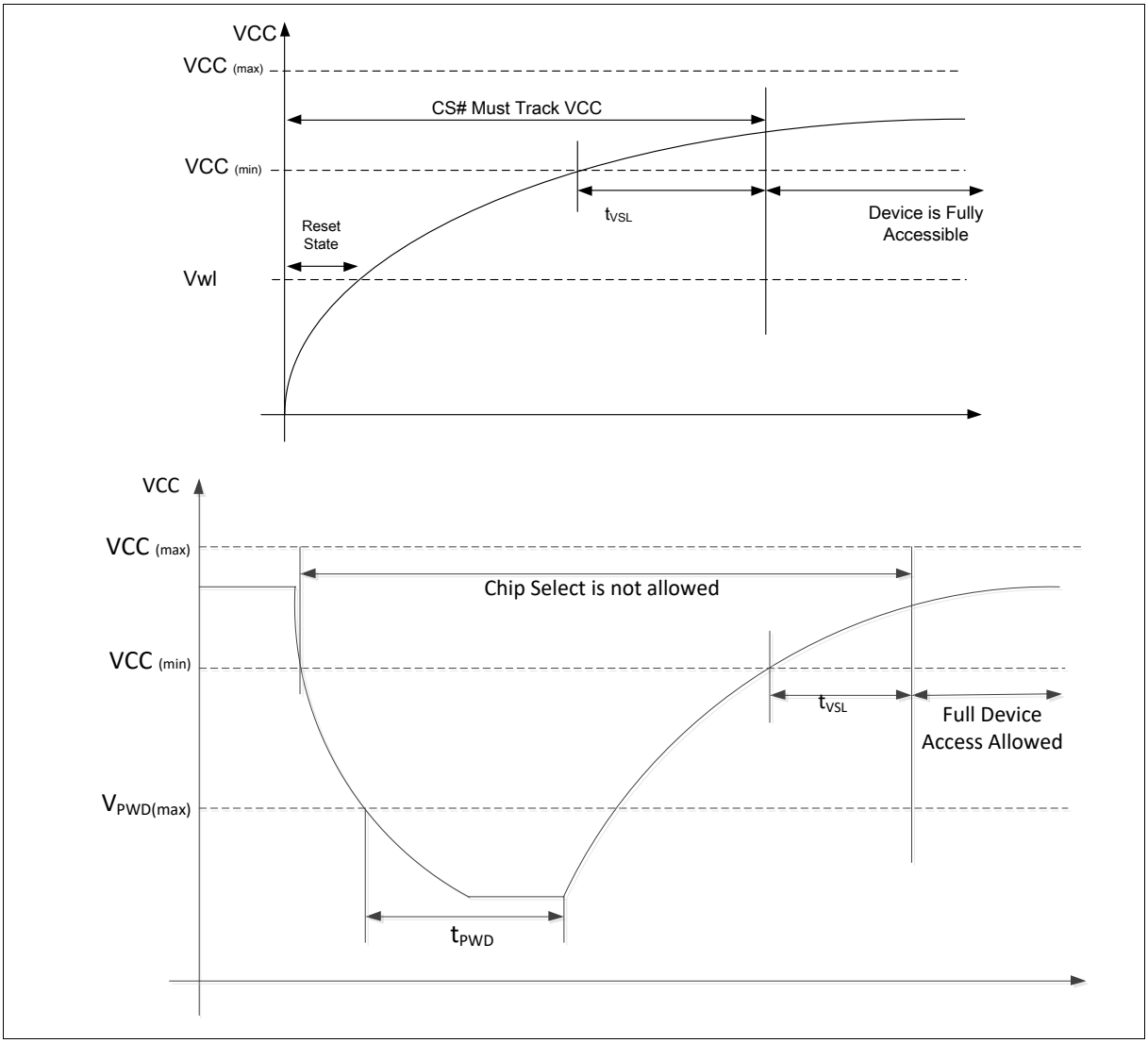


Figure 47 Power-up Timing& Power Up/Down and Voltage Drop

11.4. DC Electrical Characteristics

Table8 DC Characteristics

Applicable over recommended operating range from: T_A= -40°C to 85°C, V_{CC} = 2.7V to 3.6V,(unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Vcc	Supply Voltage		2.7		3.6	V
I_{LI}	Input Leakage Current				±2	µA
I_{LO}	Output Leakage Current				±2	µA
I_{CC1}	Standby Current	CS# = V_{CC}, V_{IN} = Vss or V_{CC}		1	5	µA
I_{CC2}	Deep Power-down Current	CS# = V_{CC}, V_{IN} = Vss or V_{CC}		1	5	µA
I_{CC3}(1)	Read Data Current (1)	CLK=0.1V_{CC}/0.9V_{CC} at 50MHz, DQ open		8	15	mA
I_{CC3}(1)		CLK=0.1V_{CC}/0.9V_{CC} at 80MHz, DQ open		10	20	
I_{CC3}(1)		CLK=0.1V_{CC}/0.9V_{CC}, at 104MHz, DQ open		12	25	mA
I_{CC4}	Operating Current (WRSR)	CS#=V_{CC}		10	15	mA
I_{CC5}	Operating Current (PP)	CS#=V_{CC}		10	15	mA
I_{CC6}	Operating Current (SE)	CS#=V_{CC}		10	15	mA
I_{CC7}	Operating Current (BE)	CS#=V_{CC}		10	15	mA
V_{IL}(2)	Input Low Voltage		-0.5		0.3V_{CC}	V
V_{IH}(2)	Input High Voltage		0.7V_{CC}		V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC}-0.2			V
V_{WI}	Write Inhibit Threshold Voltage		1.0		2.2	V

Notes:

1. Checker Board Pattern.
2. V_{IL}min and V_{IH}max are reference only and are not tested.

11.5. AC Measurement Conditions

Table9 AC Measurement Conditions

SYMBOL	PARAMETER	SPEC		UNIT
		MIN	MAX	
CL	Load Capacitance		20	pF
TR, TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	0.2 V_{CC} to 0.8 V_{CC}		V
IN	Input Timing Reference Voltages	0.3 V_{CC} to 0.7 V_{CC}		V
OUT	Output Timing Reference Voltages	0.5V_{CC}		V

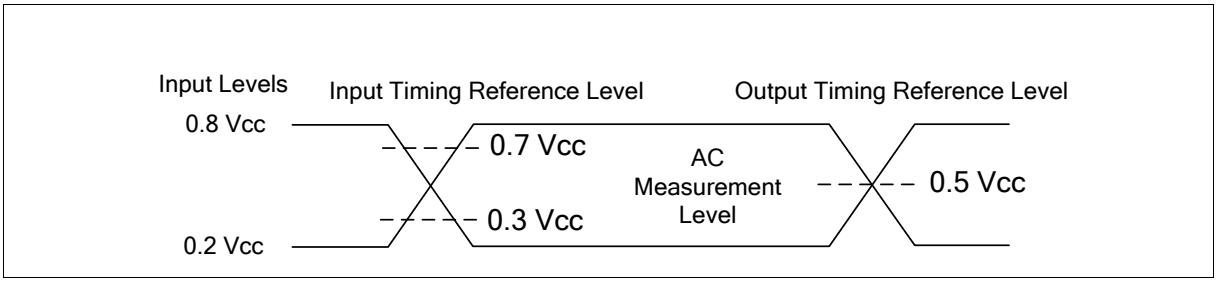


Figure 48 AC Measurement I/O Waveform

11.6. AC Electrical Characteristics

Table10 AC Characteristics

Applicable over recommended operating range from: T_A= -40°C to 85°C, V_{CC} = 2.7V to 3.6V,(unless otherwise noted).

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
F_{R1}	Serial Clock Frequency for: all commands except Read(03H) & Fast Read Quad I/O with “Continuous Read Mode”			104	MHz
F_{R2}	Serial Clock Frequency for Fast Read Quad I/O with “Continuous Read Mode”			80	MHz
f_R	Serial Clock Frequency for Read(03H)			66	MHz
t_{CH1}(1)	Serial Clock High Time	45% (1/ F_R)			ns
t_{CL1}(1)	Serial Clock Low Time	45% (1/ F_R)			ns
t_{CLCH}(2)	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CHCL}(2)	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time	20			ns
t_{SHQZ}(2)	Output Disable Time			7	ns
t_{CLQX}	Output Hold Time	1.5			ns
t_{DVCH}	Data In Setup Time	1.5			ns
t_{CHDX}	Data In Hold Time	4			ns

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
t_{HLCH}	HOLD# Low Setup Time (relative to CLK)	5			ns
t_{HHCH}	HOLD# High Setup Time (relative to CLK)	5			ns
t_{CHHH}	HOLD# Low Hold Time (relative to CLK)	5			ns
t_{CHHL}	HOLD# High Hold Time (relative to CLK)	5			ns
t_{HLQZ}(2)	HOLD# Low to High-Z Output			12	ns
t_{HHQX}(2)	HOLD# High to Low-Z Output			7	ns
t_{CLQV}	Output Valid from CLK			7	ns
t_{WHSL}	Write Protect Setup Time before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time after CS# High	100			ns
t_{DP}(2)	CS# High to Deep Power-down Mode			3	µs
t_{RES1}(2)	CS# High to Standby Mode without Electronic Signature Read			3	µs
t_{RES2}(2)	CS# High to Standby Mode with Electronic Signature Read			1.8	µs
t_{SUS}(2)	CS# High to next Instruction after Suspend			30	µs
t_{RST}(2)	CS# High to next Instruction after Reset			40	µs
t_W	Write Status Register Cycle Time		5	15	ms
t_{BP}	Byte Program Time		60	100	µs
t_{PP}	Page Program Time		0.4	2.5	ms
t_{SE}	Sector Erase Time		30	300	ms
t_{BE}	Block Erase Time (32KB)		150	1500	ms
t_{BE}	Block Erase Time (64KB)		200	2000	ms
t_{CE}	Chip Erase Time		25	60	s

Notes:

1. $t_{CH}+t_{CL} >= 1 / F_R$ or $1/f_R$;
2. This parameter is characterized and is not 100% tested.

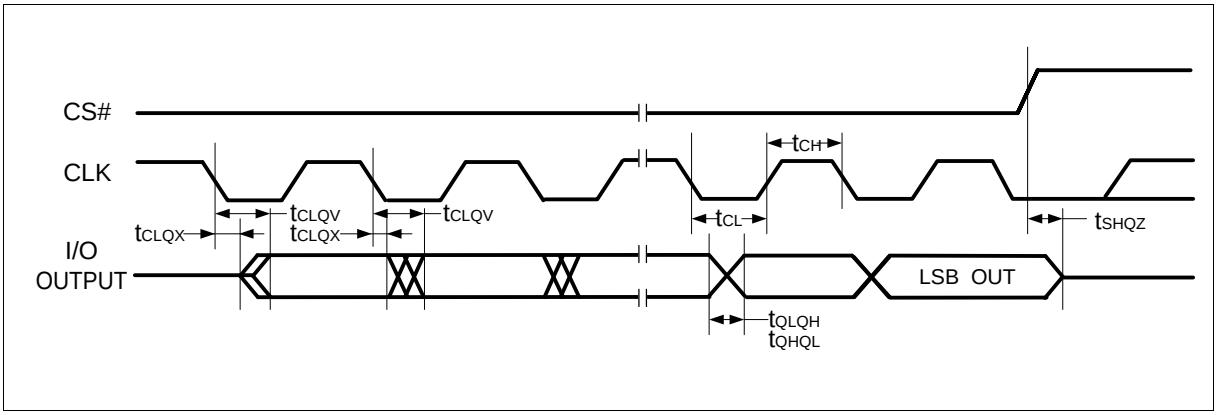


Figure 49 Serial Output Timing

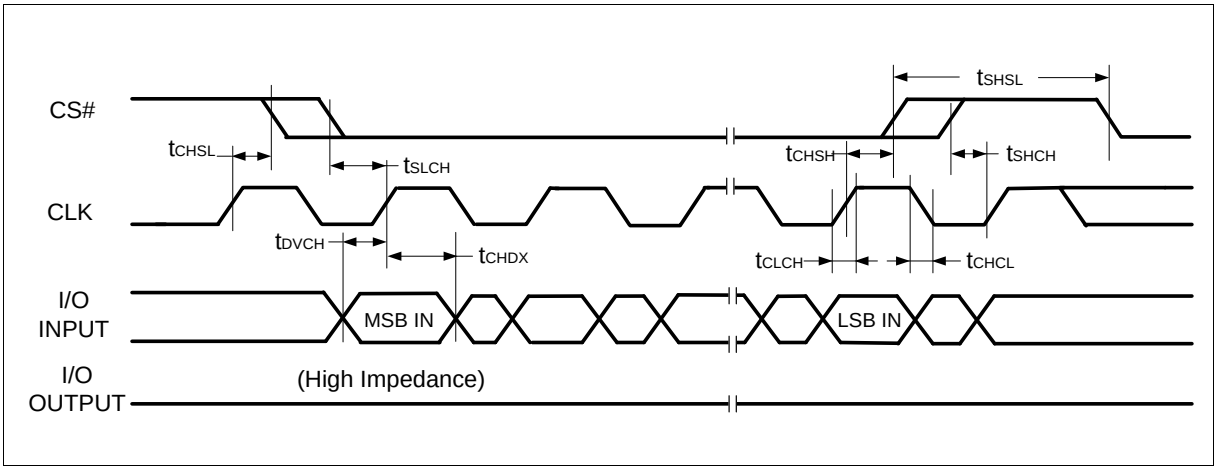


Figure 50 Serial Input Timing

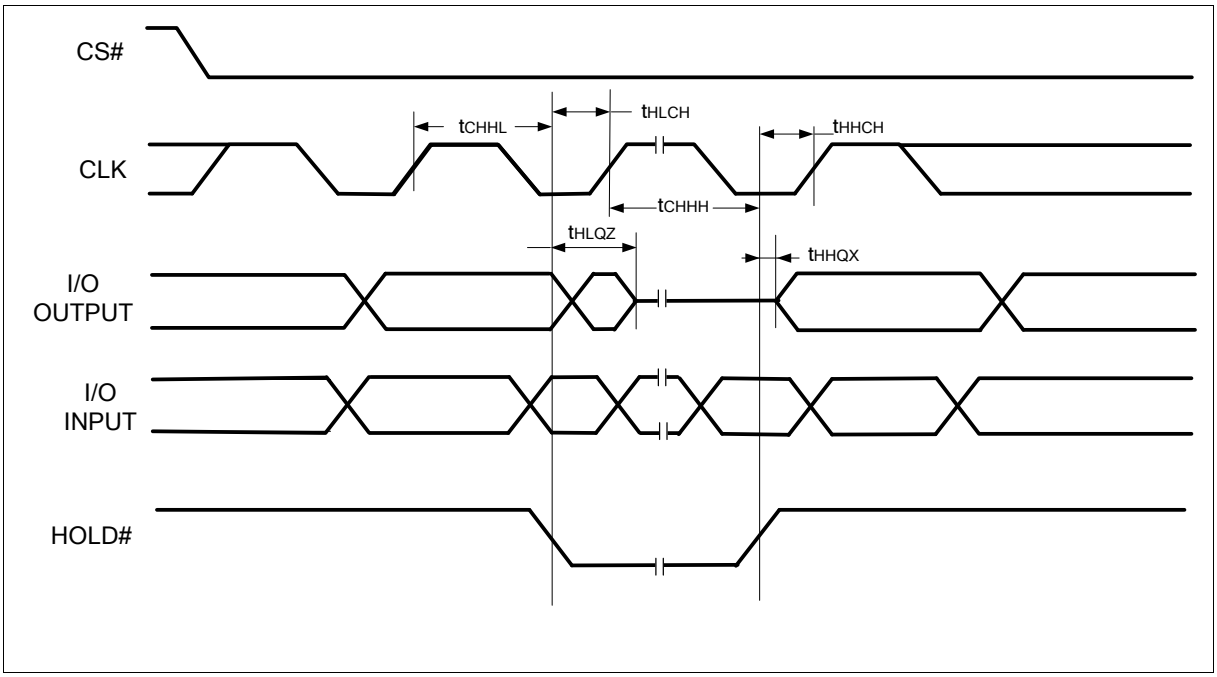


Figure 51 Hold Timing

12. Ordering Information

FM 25Q 64A I3 -XXX-C-H M -OP

Company Prefix

FM = Fudan Microelectronics Group Co.,ltd

Product Family

25Q = 2.7~3.6V Serial Flash with 4KB Uniform-Sector, Dual/Quad SPI & QPI

Product Density

64A = 64M-bit

Temperature Range

I3 = Industrial: -40℃ to 85℃

Package Type

SO = 8-pin SOP (150mil)
SOB = 8-pin SOP (208mil)
DNA = 8-pin TDFN (5x6mm)
USA = 8-pin USON (4x3mm)
BGB = 24-ball BGA (8x6mm)

Product Carrier

U = Tube
T = Tape and Reel
A = Tray

HSF ID Code

G = RoHS Compliant, Halogen-free, Antimony-free

MSL Level

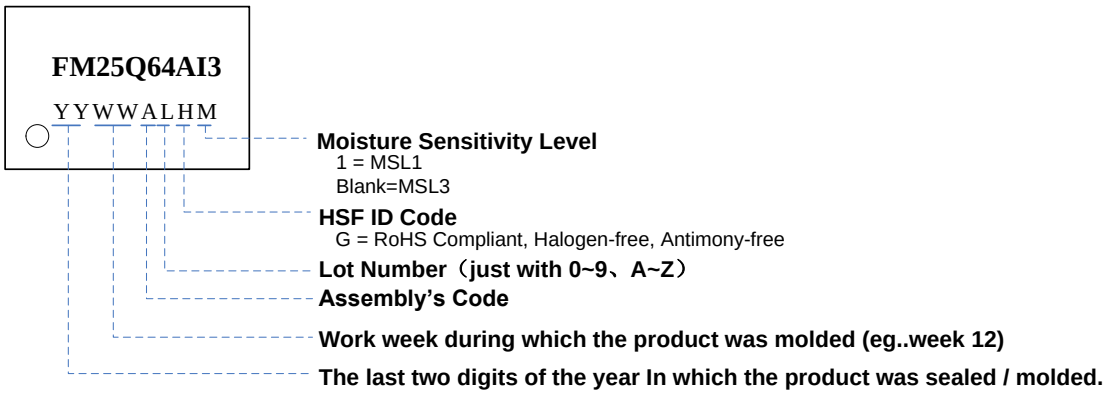
1 = MSL1
3 = MSL3

OPTION

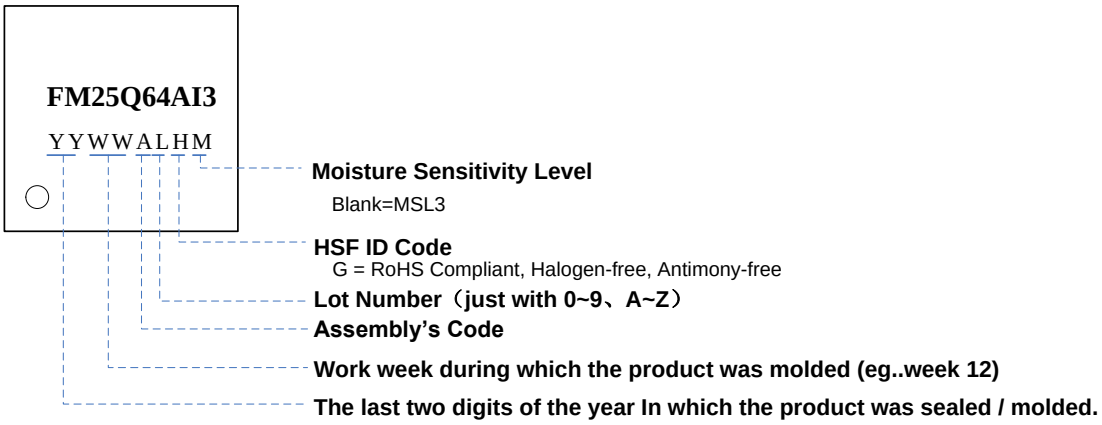
Blank = SR1/2 factory default value is 00/00.
S1 = SR1/2 factory default value is 80(SR1)/03(SR2), Status Register is permanently protected.

13. Part Marking Scheme

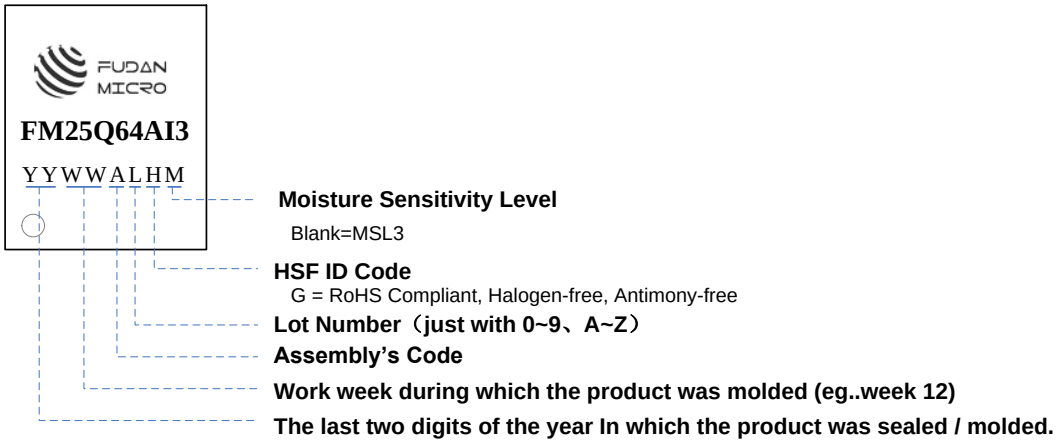
13.1. SOP8 (150mil)



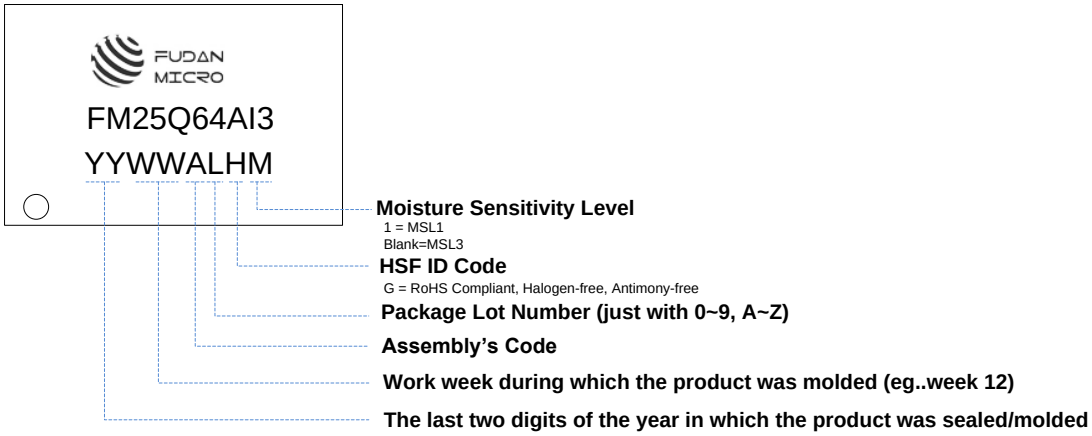
13.2. SOP8 (208mil)



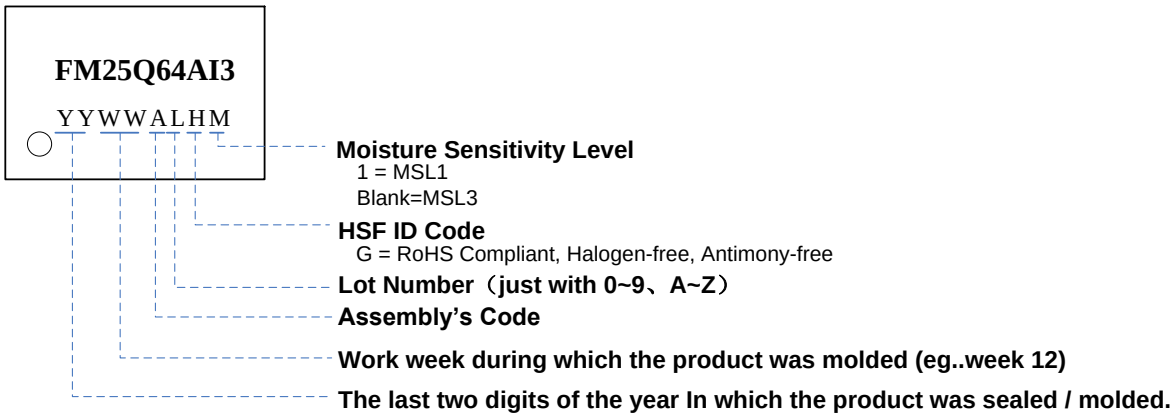
13.3. TDFN8 (5x6mm)



13.4. BGA24 (8x6mm) (5x5 Ball Array)

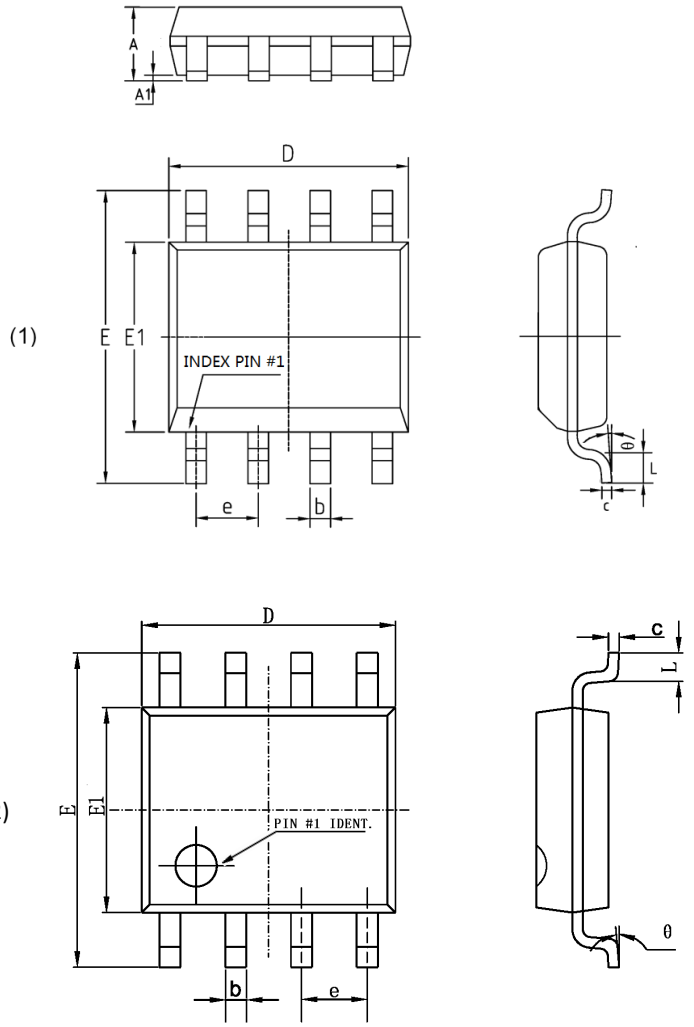


13.5. USON8 (4x3mm)



14. Packaging Information

SOP8 (150mil)

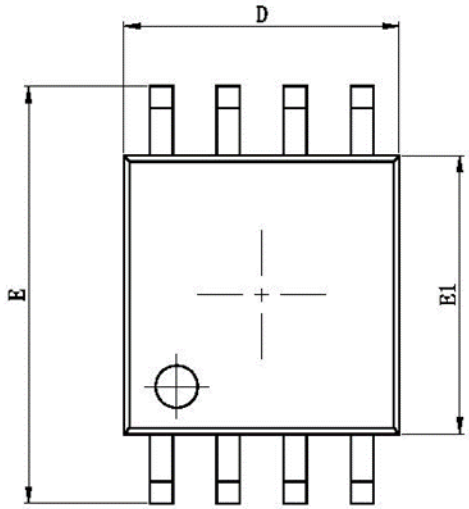


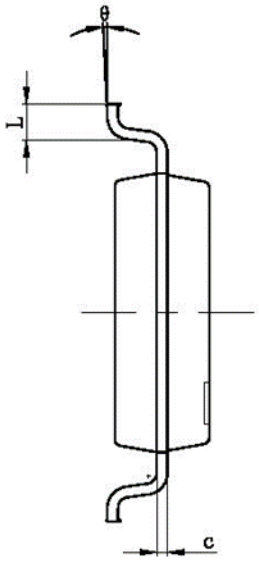
Symbol	MIN	NOM	MAX
A	1.350	1.550	1.750
A1	0.050	0.150	0.250
b	0.330	0.420	0.510
c	0.150	0.200	0.250
D	4.700	4.925	5.150
E1	3.700	3.900	4.100
E	5.800	6.000	6.200
e	1.270(BSC)		
L	0.400	0.650	0.900
θ	0°	4°	8°

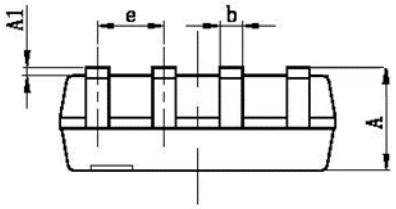
NOTE:

1. **Dimensions are in Millimeters.**

SOP8 (208mil)





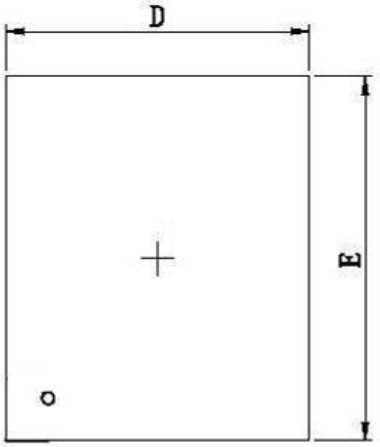


Symbol	MIN	NOM	MAX
A	1.750	1.950	2.150
A1	0.050	0.150	0.250
b	0.350	0.425	0.500
c	0.100	0.175	0.250
D	5.130	5.230	5.330
E1	5.180	5.280	5.380
E	7.700	7.900	8.100
e	1.270(BSC)		
L	0.500	0.675	0.850
θ	0°	4°	8°

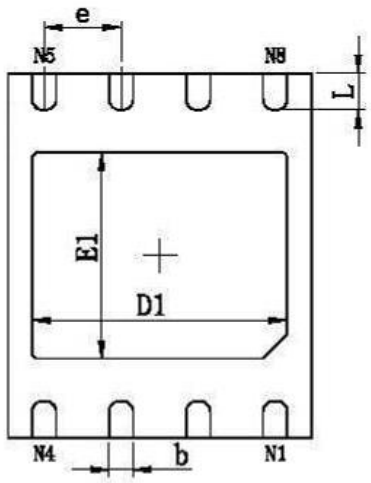
NOTE:

1. **Dimensions are in Millimeters.**

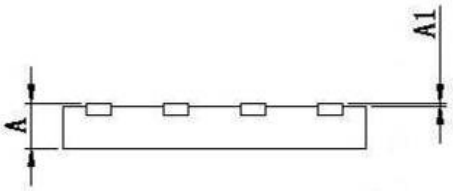
TDFN8 (5x6mm)



Top View



Bottom View



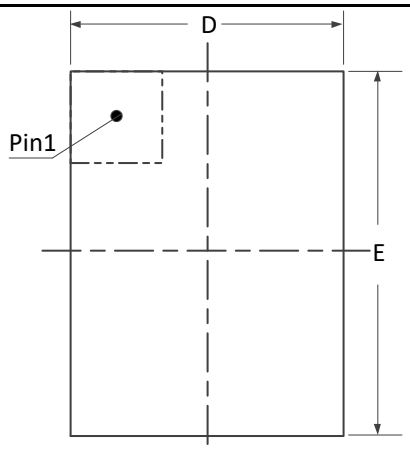
Side View

Symbol	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	0.025	0.050
D	4.900	5.000	5.100
D1	3.900	4.150	4.400
E	5.900	6.000	6.100
E1	3.300	3.400	3.500
b	0.350	0.400	0.450
e	1.270TYP		
L	0.500	0.600	0.700

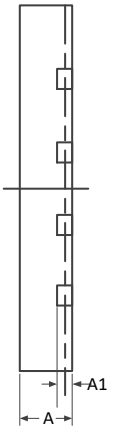
NOTE:

1. **Dimensions are in Millimeters.**

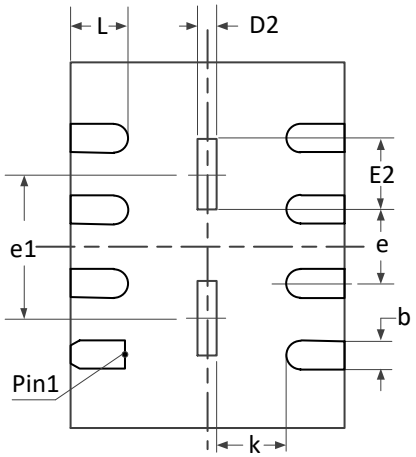
USON8(4x3mm)



TOP VIEW



SIDE VIEW



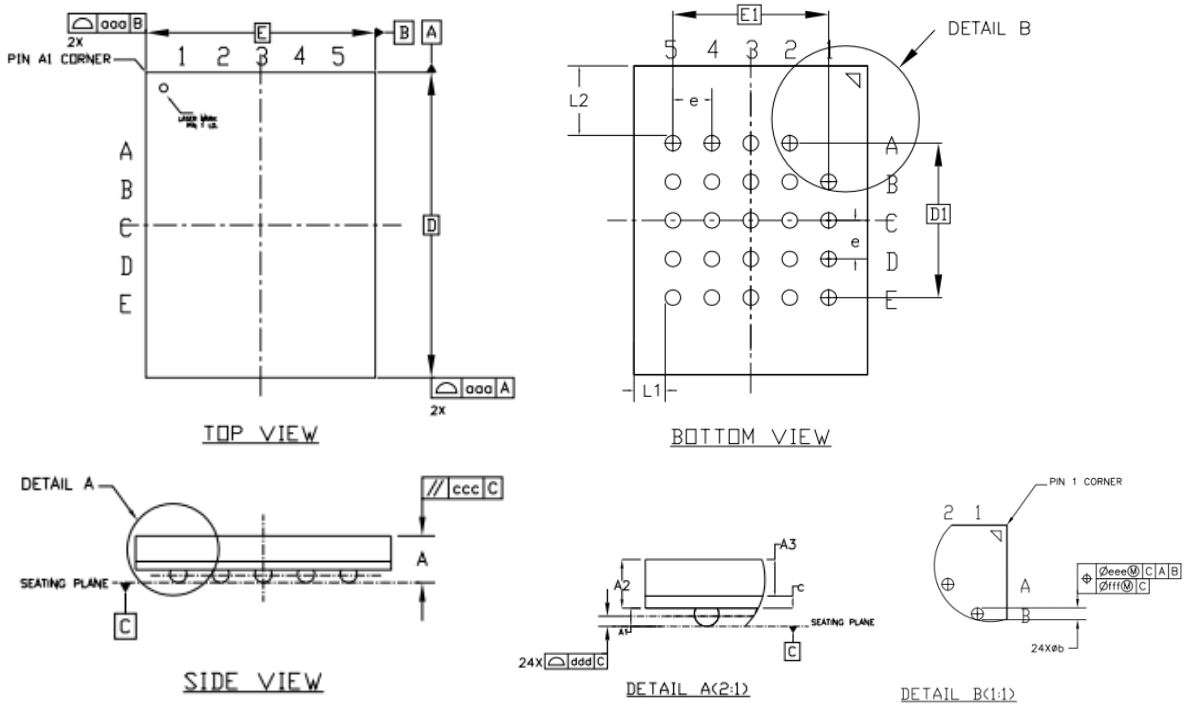
BOTTOM VIEW

Symbol	MIN	NOM	MAX
A	0.500	0.550	0.600
A1		0.150 REF	
D		3.000 BSC	
E		4.000 BSC	
D2	0.100	0.200	0.300
E2	0.700	0.800	0.900
k		0.800 REF	
b	0.200	0.275	0.350
e		0.800 BSC	
e1		1.600 BSC	
L	0.500	0.600	0.700

NOTE:

1. **Dimensions are in Millimeters.**

BGA24 (8x6mm) (5x5 Ball Array)



Symbol	MIN	NOM	MAX
A	---	---	1.200
A1	0.250	0.300	0.350
A2		0.790 BSC	
D	7.900	8.000	8.100
D1		4.000 BSC	
E	5.900	6.000	6.100
E1		4.000 BSC	
e		1.000 BSC	
b	0.350	0.400	0.450

Note:
1. Dimensions are in Millimeters.

15. Revision History

VERSION	DATE	PAGE	Revise Description
Preliminary	Apr.2022	67	Initial Document Release.
1.0	Aug.2022	67	Update DC/AC Electrical Characteristics
1.1	Feb.2024	67	Fix some clerical errors
1.2	May.2024	70	Update BGA24 packaging information. Add ordering information OP item.
1.3	Sep.2024	70	Update POD、ordering information

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